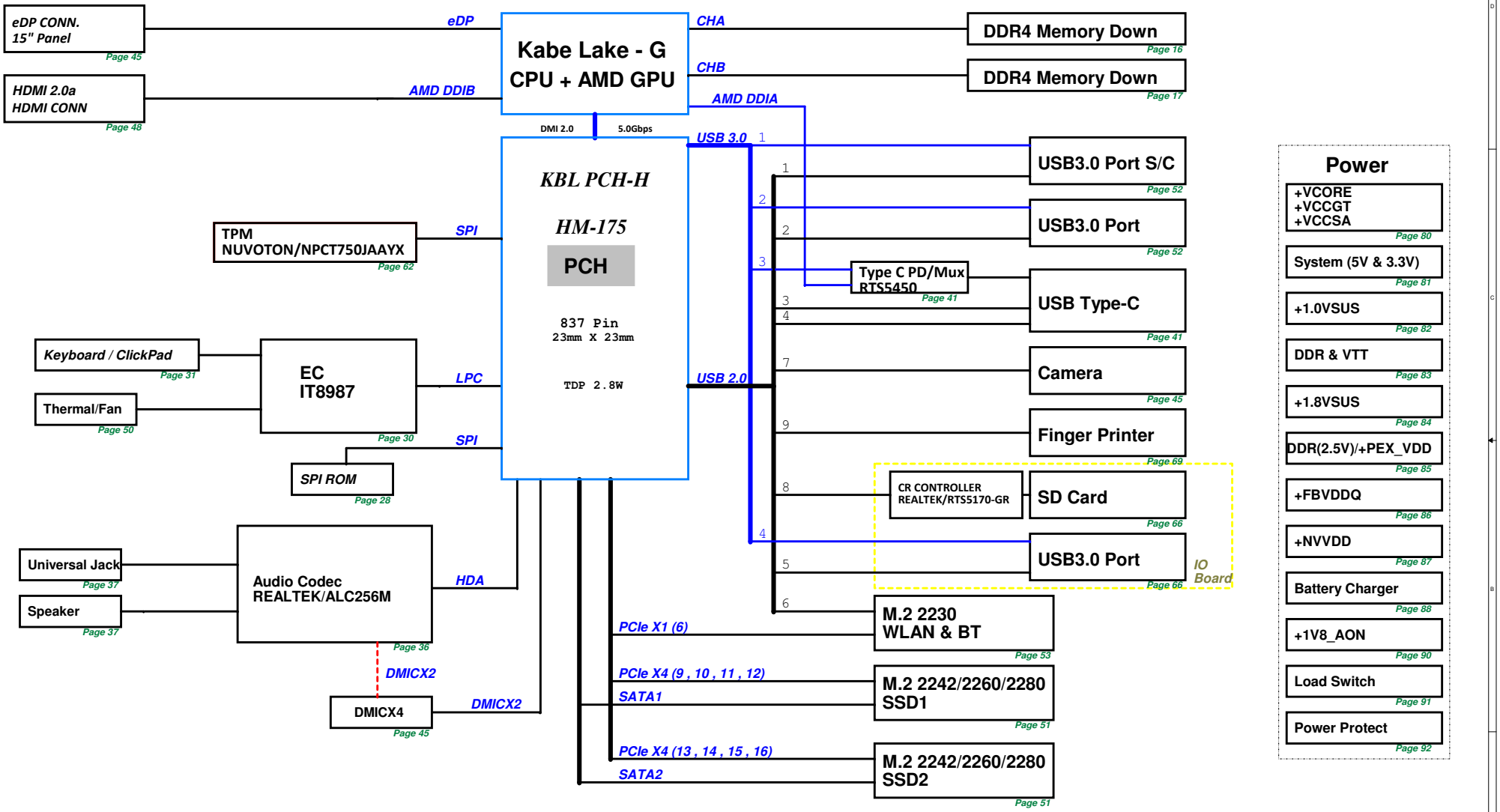
GS5FA Block Diagram



PEGATRON Title : Block Diagram

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 1 of 98

Option

Optional	Remark
/2MIC	Support 2MIC
/4MIC	Support 4MIC
/CHB	Only Memory CHB
/DDP	Support DDP Memory
/SDP	Support SDP Memory
/Debug	Debug only
/Dead Battery	Support Dead Battery function
/EMI	EMI Solution
/TEST	AUTO TEST For AC
/TPANEL	Support Touch Panel function
/TPM	Support TPM function
/USBSLP	
@	Unmount
@/Dead battery	Support TPM function
@/EMI	Unmount EMI Solution
@/SP	Short Pin
@/TPM	Unmount TPM
@WiFi5G	

PEGATRON Title : Option

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BG1/HW1 Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

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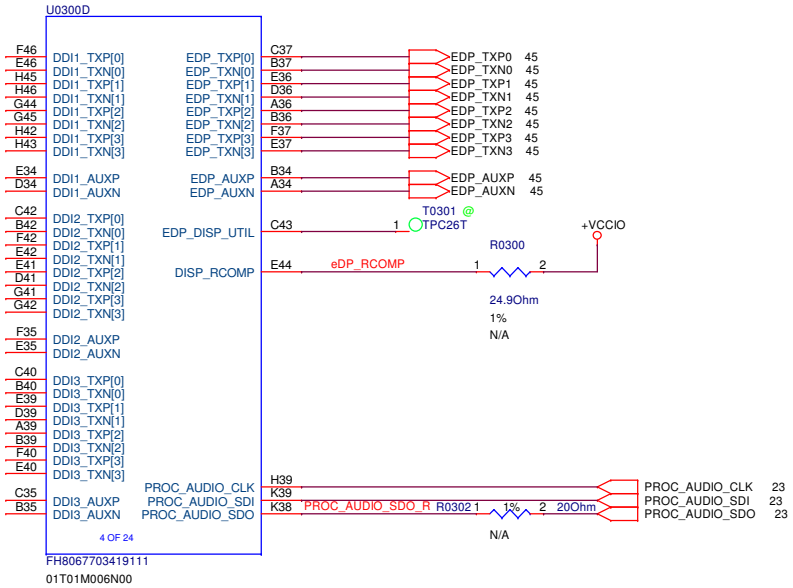
03 CPU(1) DDI/EDP

+VCCIO +VCCIO 5,9,57,94



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Title : CPU DDI/EDP

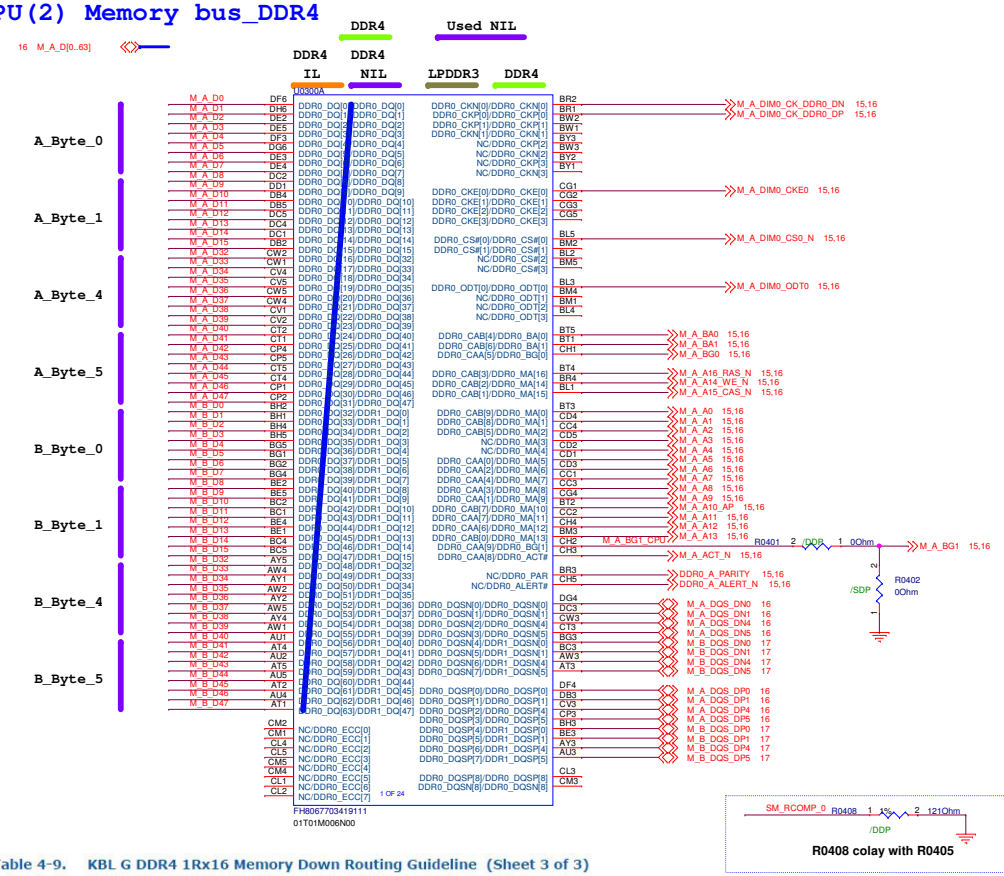
BG1/HW1

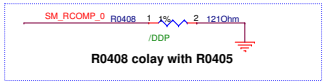
Engineer: James Liao

Size	Project Name	Rev
A3	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 3 of 98

04 CPU(2) Memory bus_DDR4





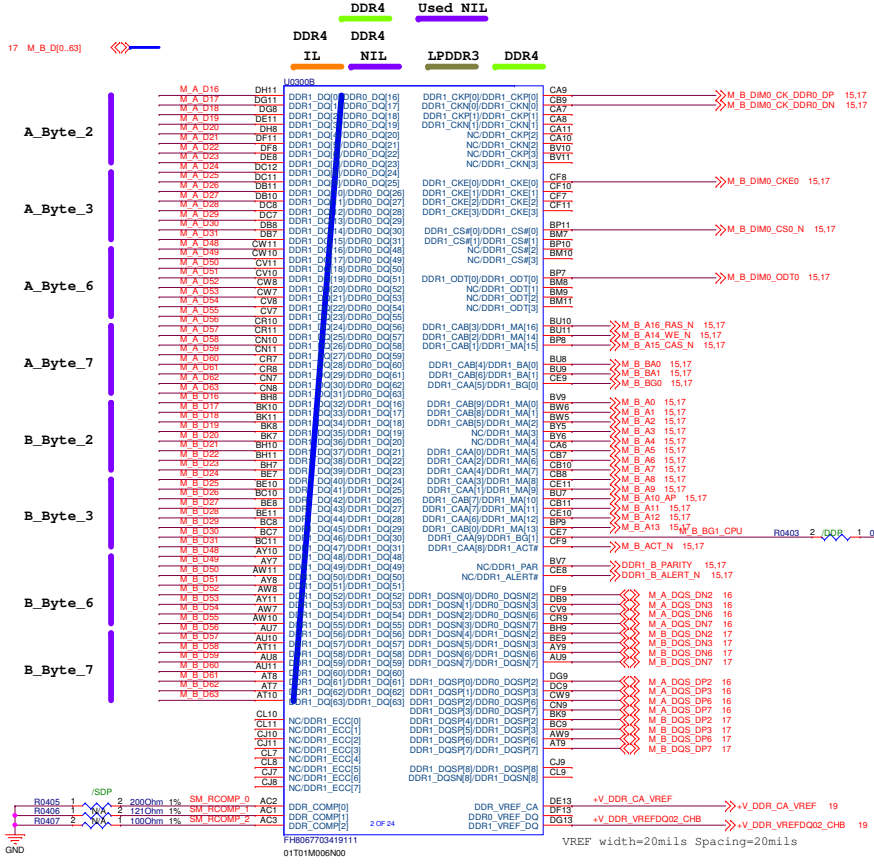


Table 4-9. KBL G DDR4 1Rx16 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max (mils) Length			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group[1&2]	Byte [1&2]	Region	Breakout	Total		

Notes:

1. Avoid any parallel routing between two adjacent layers. When parallel routing can not be avoided in the CPU Break Out, it is recommended to offset the signals from two adjacent layers so no direct overlap occurs. If needed, the total parallel routing length in the CPU Break Out, which includes both overlapped and offset parallel routing, must be 300 mils or less.
2. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
3. Use individual termination resistors (R1) for each signal. Don't use Rpacks
4. For Option #1 (Single Rank) configuration there are only 8 DRAM Devices connected to each CMD Group Signal and only 1 DRAM Device connected to each Strobe/Data Group Signal. For these designs DRAM Devices [15:8] and their corresponding BI1 routing segments need to be removed for each CMD Group Signal and the second DRAM Device and corresponding BI routing segment needs to be removed for each Strobe/Data Group Signal.
5. The Strobe and Data Group Signals within the same byte must always route together on the same layers for their entire route
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
7. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed
8. Capacitor C1 is a defensive design and should be NO STUFF by default
9. DQ and DQS signals must route at the same layer and have same width
10. Route 2 adjacent bytes to same DRAM device - like DRAM0(BYTE0,1) DRAM1 (BYTE 2,3),,, for better VREF training per DRAM device.
11. Impedance numbers are for reference only, it is calculating according to the stackup layers thickness, the material conductivity, traces spacing and width. The recommendation is to follow stackup and traces geometries.
12. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm

RCOMP [0]	M	MS/ DSL	VSS	4	12-15					13	13		500		500	200/ 121	12
RCOMP [1]	M	MS/ DSL	VSS	4	12-15					13	13		500		500	121	
RCOMP [2]	M	MS/ DSL	VSS	4	12-15					13	13		500		500	100	

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Title: CPU_SYS_POWER_MANAGER

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

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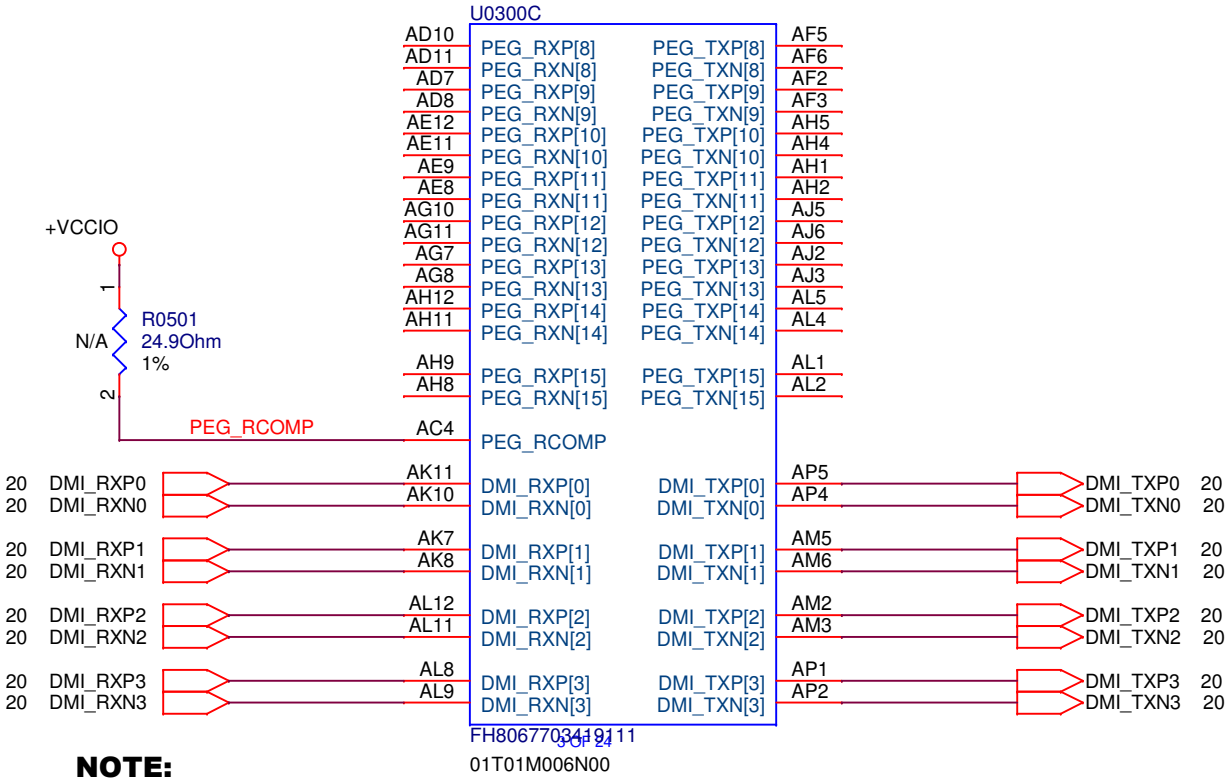
05 CPU(3) DMI

+VCCIO +VCCIO 3,9,57,94



NOTE:

W/S=12/15 mil, length<400mil

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Title: CPU DMI

BG1/HW1

Engineer: James Liao

Size	Project Name	Rev
A	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 5 of 98

06 CPU(4) CFG

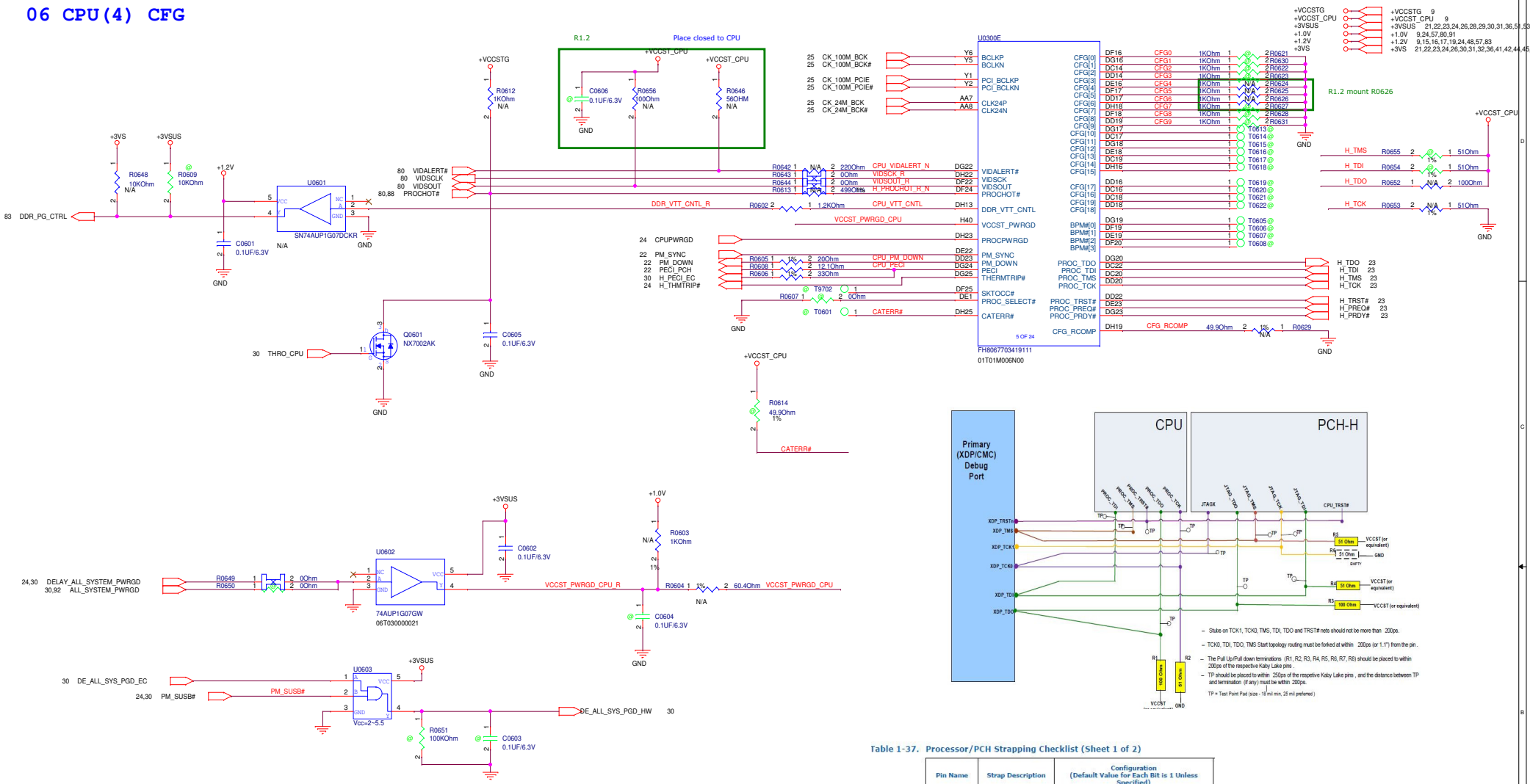

Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted. — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** Should be set to 1 • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[5]:** Should be set to 0 • **CFG[6]:** PCI Express* Bifurcation — 0 = 2x4 PCI Express* — 1 = 1x8 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	• CFG[2], CFG[6:5] and CFG[7] are relevant for G-Processor Line and test point may be placed on the board for them.

Table 1-37. Processor/PCH Strapping Checklist (Sheet 1 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.
CFG[1]	Reserved. No connect	
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation 0 = Lane numbers reserved
CFG[3]	Reserved configuration lane	
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express* Recommend 1K Ω ±5% pull-down resistor to GND.
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.
CFG[19:8]	Reserved configuration lands.	

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Title : CPU CFG

Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

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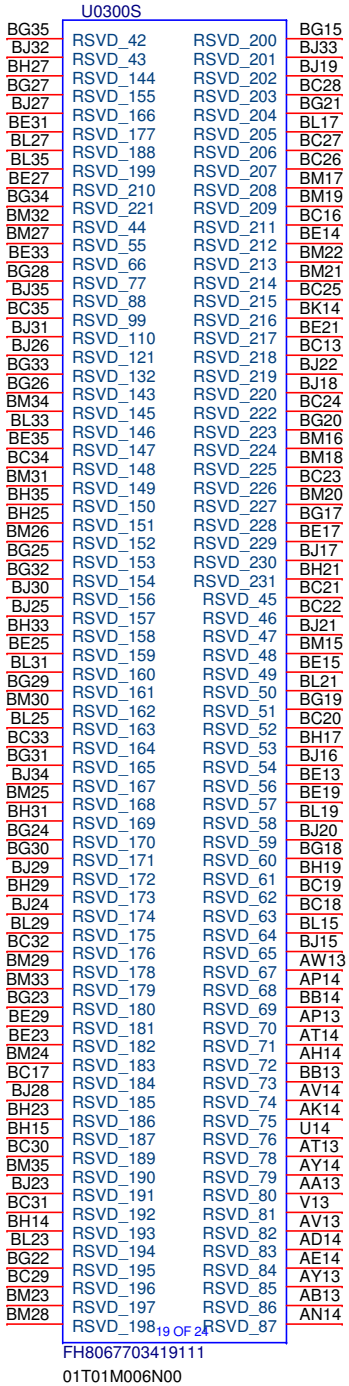
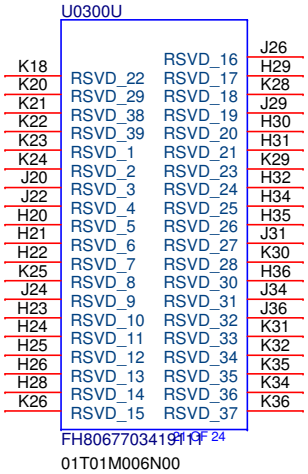
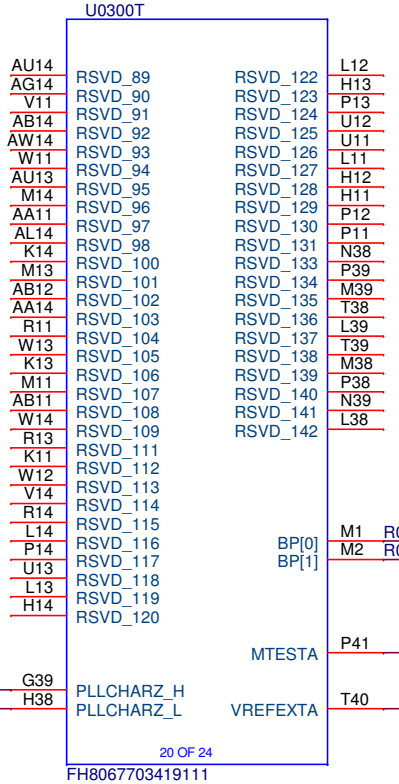
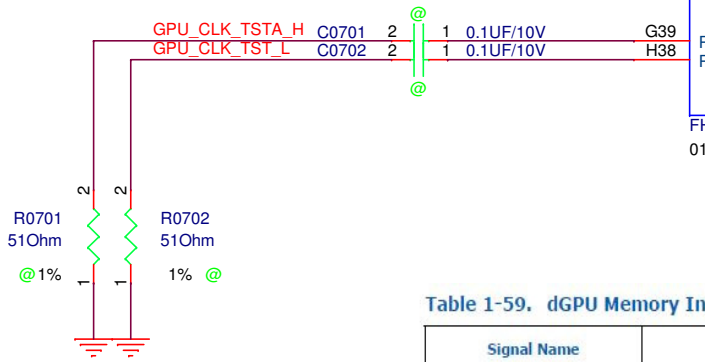
07 CPU(5) RSVD









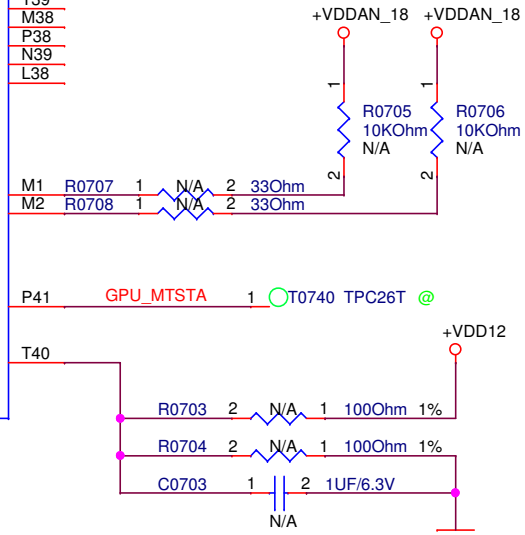


Table 1-59. dGPU Memory Interface (HBM)

Signal Name	Description	Dir.	Link Type
VREFEXTA	External voltage reference for HBM. 0.5 × CHA_VDD12 Two 100-Ω 1% resistors can be used to form the divider on each pin. Filter capacitor is needed to ensure AC noise is within ±10 mV.	I	SE
MTESTA	Reserved. Provide test pads on the PCB.	I/O	SE

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BGT/HW1

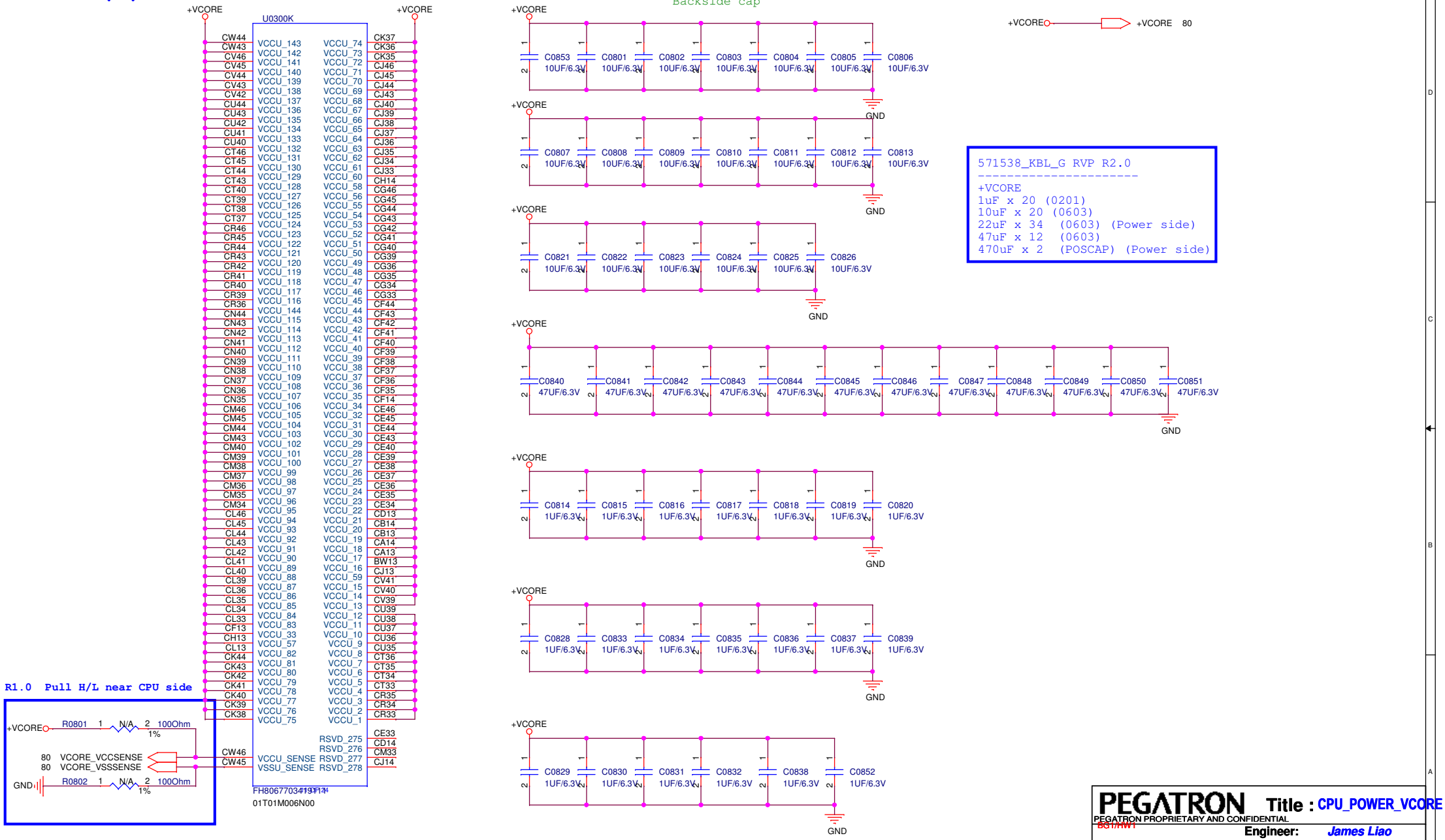
Title : CPU_RSVD

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 7 of 98

08 CPU(6) POWER VCORE



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BG1/HW1

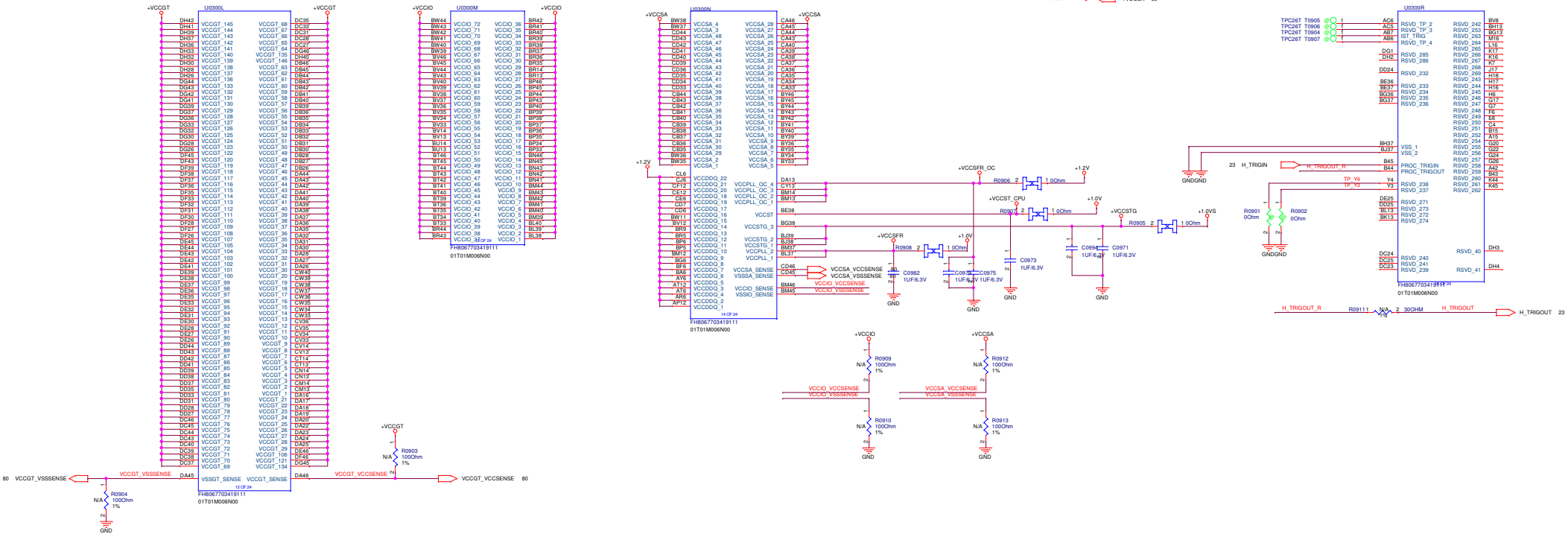
Title : CPU_POWER_VCORE

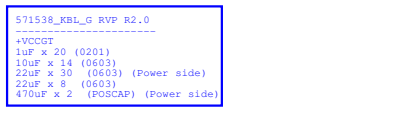
Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 8 of 98

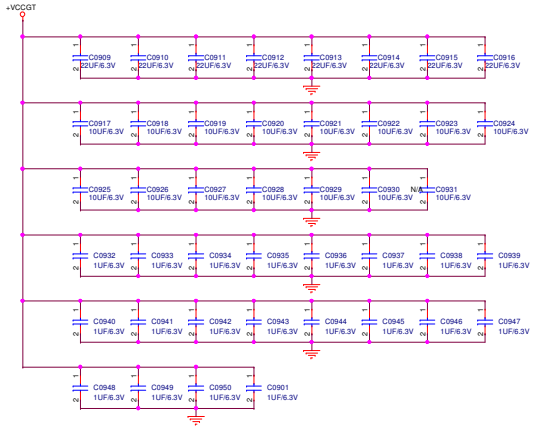
09 CPU(7) POWER GT_IO_SA





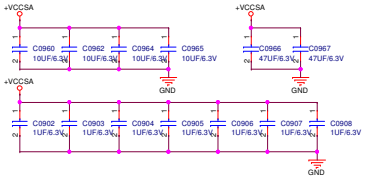
571538_KBL_G RVP R2.0

+VCCGT
1uF x 20 (0201)
10uF x 14 (0603)
22uF x 30 (0603) (Power side)
22uF x 8 (0603)
470uF x 2 (POSCAP) (Power side)



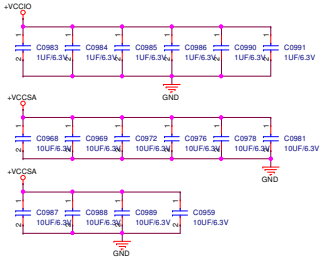
571538_KBL_G RVP R2.0

+VCCSA
1uF x 7 (0201)
10uF x 4 (0603)
22uF x 9 (0603) (Power side)
47uF x 2 (0603)



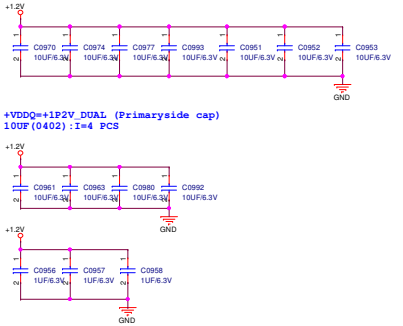
571538_KBL_G RVP R2.0

+VCCIO
1uF x 6 (0402)
10uF x 10 (0603)
22uF x ?? (0603) (Power side)
47uF x ?? (0805) (Power side)
470uF x ?? (POSCAP) (Power side)



571538_KBL_G RVP R2.0

+1.2V (VCCDDQ)
1uF x 3 (0402)
10uF x 11 (0603)
22uF x 6 (0603) (Power side)



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Title: CPU_POWER_GT_IO_SA

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 9 of 98

PEGATRON

Title : CPU_POWER_04

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Engineer: James Liao

Size	Project Name	Rev
A3	GS5FA	1.0

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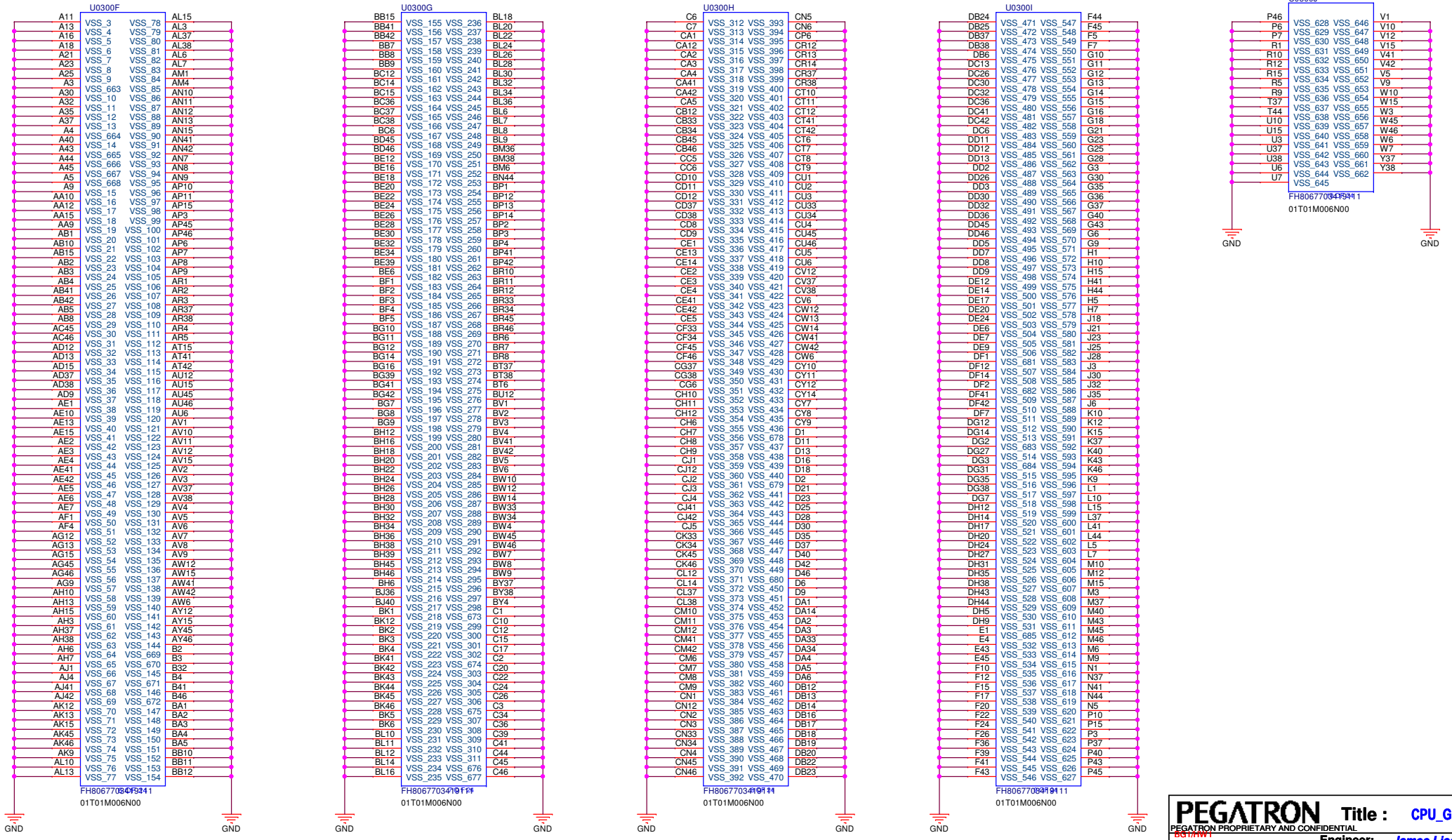
11 CPU(8) GND



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Title : CPU_GND

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 11 of 98

PEGATRON Title :

Engineer: James Liao

Size: A | Project Name: G65FA | Rev: 1A

Date: [illegible] Sheet [illegible] of [illegible]

PEGATRON Title :<Title>

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BG1-HW1

Engineer: James Liao

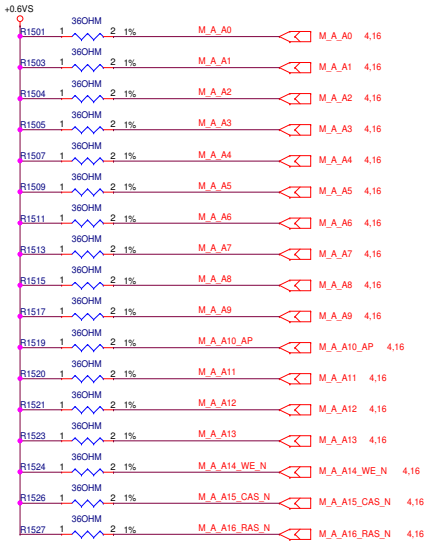
Size	Project Name	Rev
Custom	GS5FA	1.0

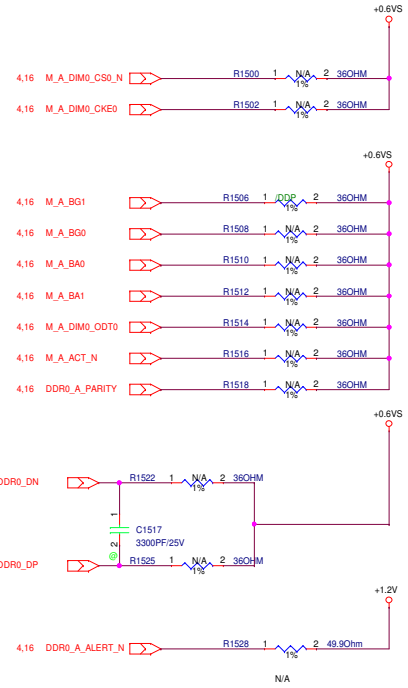
Date: Monday, December 10, 2018 Sheet 13 of 98

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	14 of 98

15 DDR4(0)_Termination

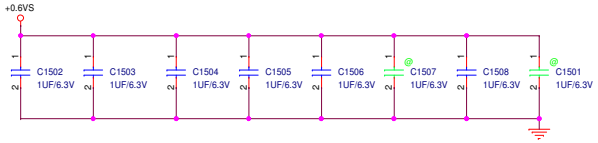
CHA

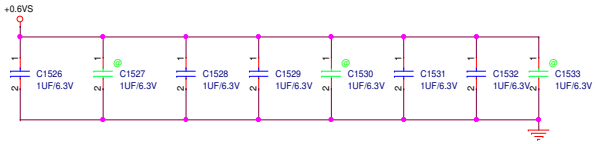


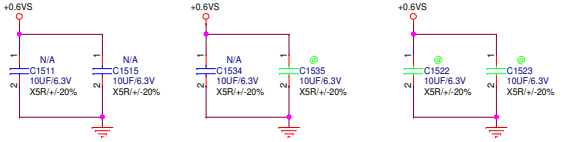


+0.6VS +1.2V — +0.6VS 57,83 +1.2V 6,9,16,17,19,24,48,57,83

Average placed close to +VDDQ_VTT power plane







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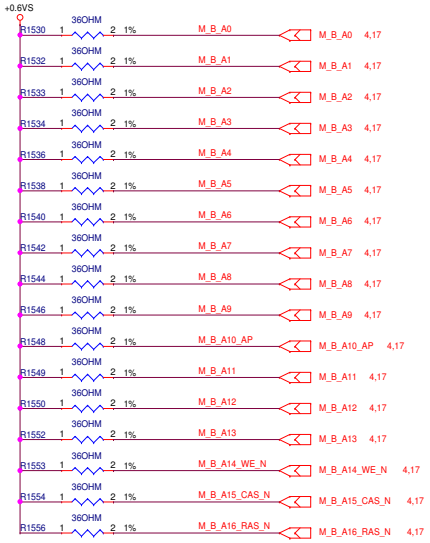

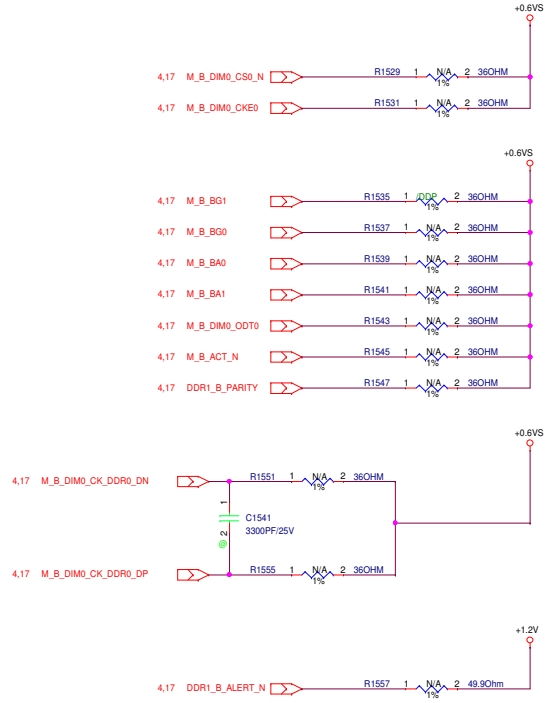

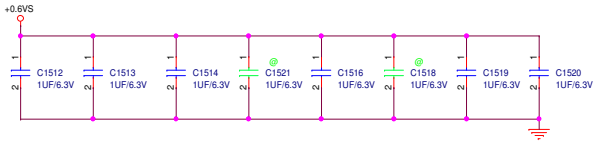

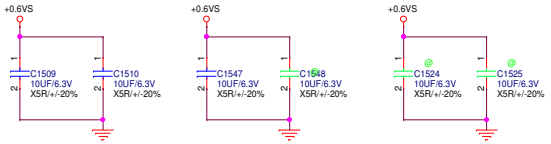

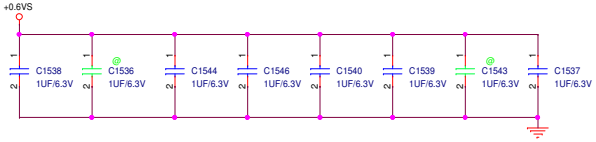

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<Org Name>

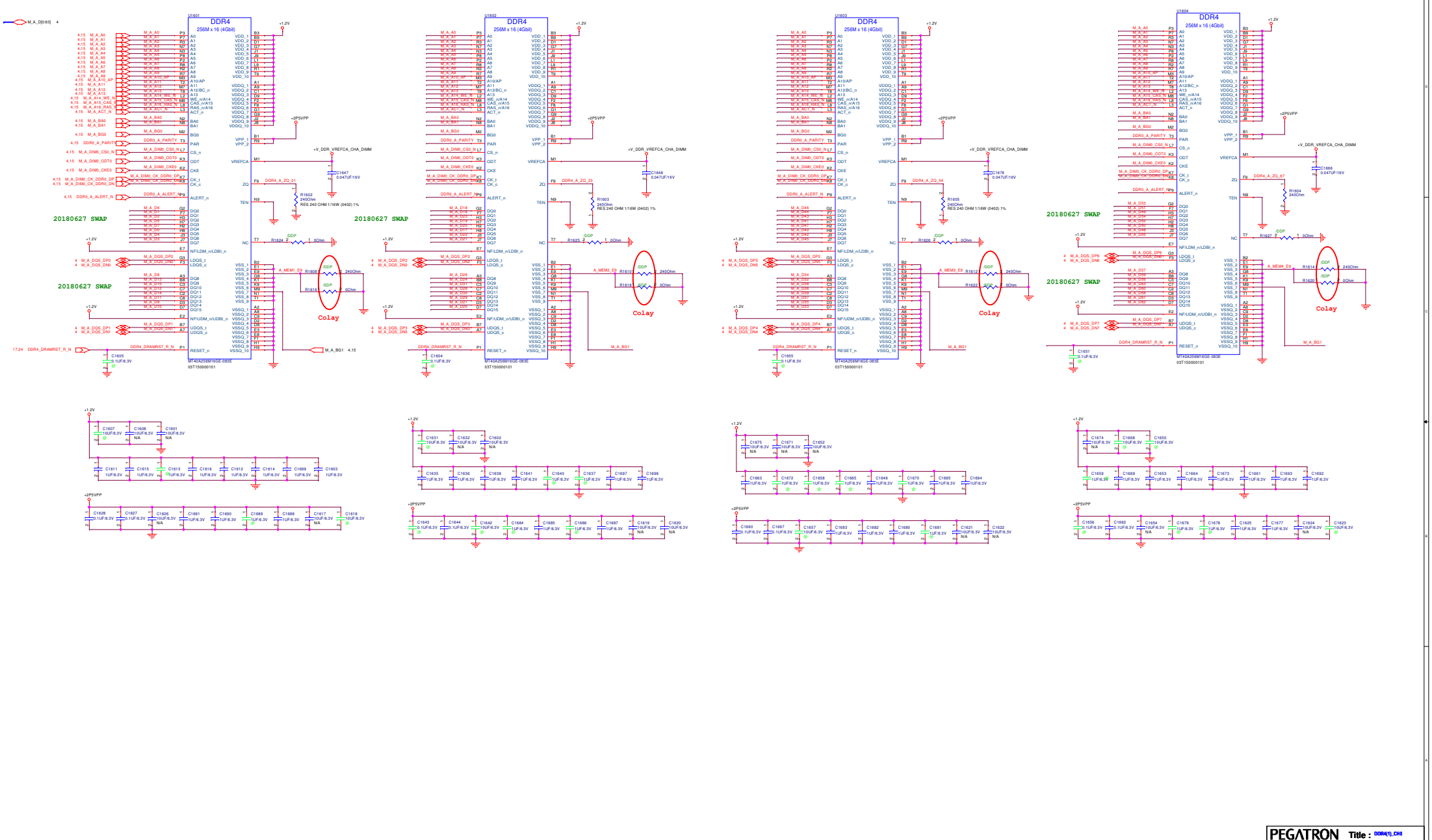
Title : DDR4(0)_Termination

Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 15 of 98

16 DDR4(1)_CH0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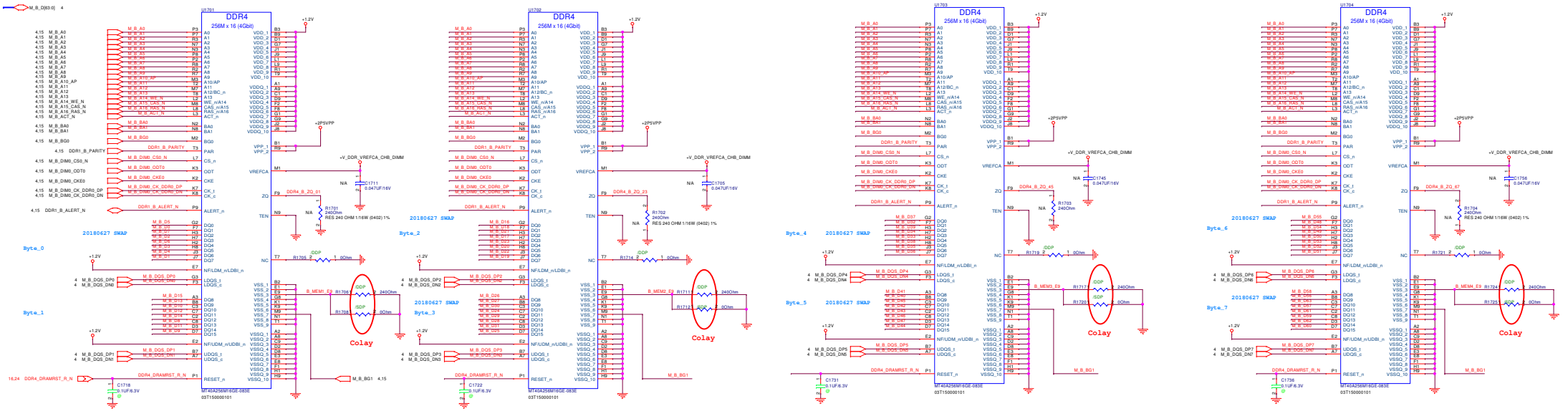
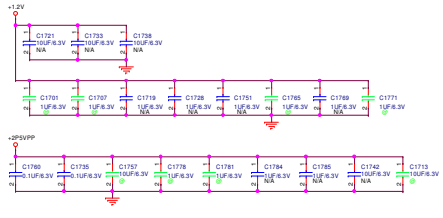
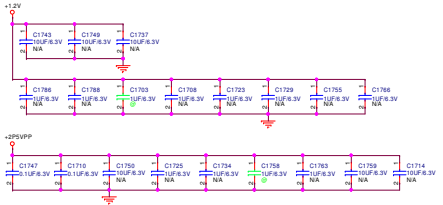
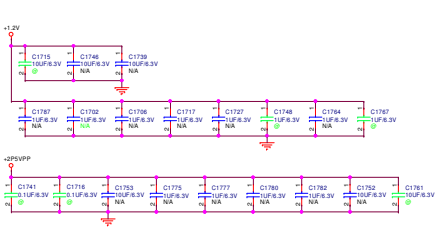
03T1500000101

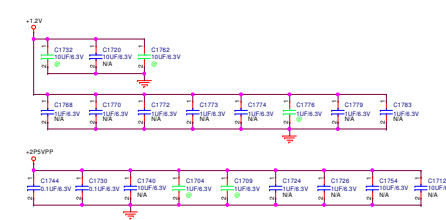
17 DDR4(2)_CH1











PEGATRON	Title : DDR4(2)_CH1		
PROPRIETARY AND CONFIDENTIAL	Engineer: James Liao		
Size: D	Project Name: GS5FA		Rev: 1.0
Date: Monday, December 10, 2018	Sheet 17 of 98		

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	18 of 98

19 DDR4(3)_CA/DQ Voltage

+1.2V → +1.2V 6,9,15,16,17,24,48,57,83
+V_DDR_VREFCA_CHB_DIMM → +V_DDR_VREFCA_CHB_DIMM 17
+V_DDR_VREFCA_CHA_DIMM → +V_DDR_VREFCA_CHA_DIMM 16

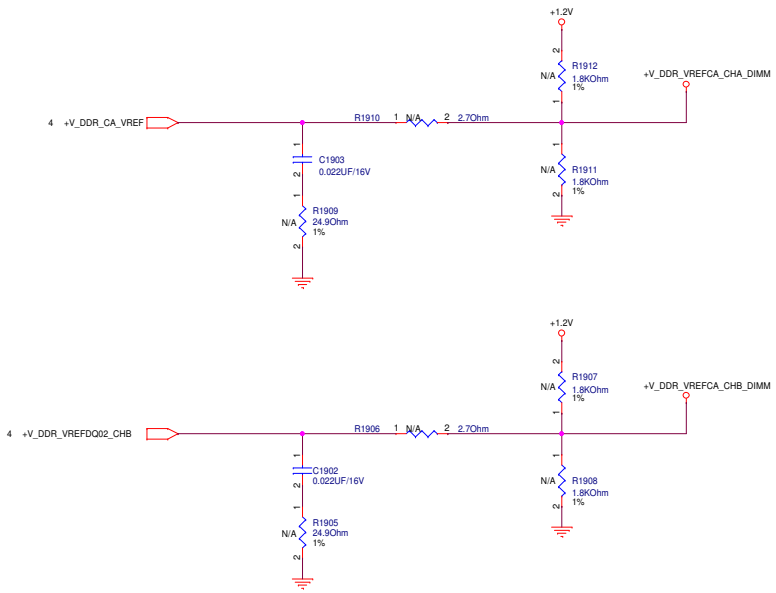
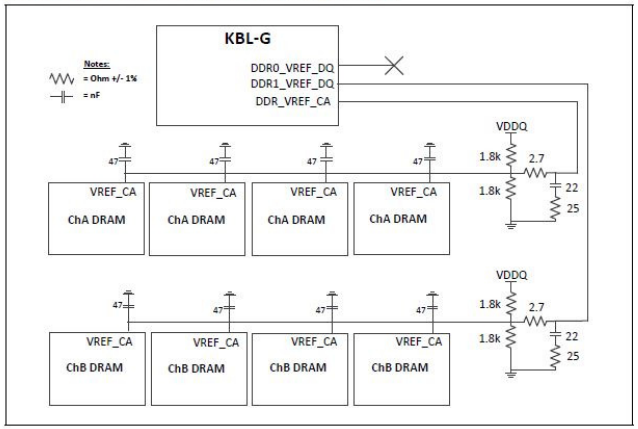


Figure 4-14. KBL G DDR4 x16 Memory Down V_{REF-CA} Overview



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>
Title : DDR4(3)_CA/DQ Voltage
Engineer: James Liao
Size C | Project Name GS5FA | Rev 1.0
Date: Monday, December 10, 2018 | Sheet 19 of 98

20 PCH(1) DMI/USB/PCIE/SATA

HM175			Grolsch
Lane1	USB3 Port1		
Lane2	USB3 Port2		USB3 (MB) (S/C)
Lane3	USB3 Port3		USB3 (MB)
Lane4	USB3 Port4		USB3 (I/O)
Lane5	USB3 Port5		USB3 (Type C)
Lane6	USB3 Port6		
Lane7	USB3 Port7	PCIe Port1	
Lane8	USB3 Port8	PCIe Port2	
Lane9		PCIe Port3	M.2 WLAN(PCIE)
Lane10		PCIe Port4	
Lane11		PCIe Port5	
Lane12		PCIe Port6	
Lane13		PCIe Port7	
Lane14		PCIe Port8	
Land15	SATA3 Port0	PCIe Port9	M.2 SSD (SATA)
Lane16	SATA3 Port1	PCIe Port10	M.2 SSD (PCIE x4)
Lane17		PCIe Port11	
Lane18		PCIe Port12	
Lane19	SATA3 Port0	PCIe Port13	M.2 SSD (PCIE x4)
Lane20	SATA3 Port1	PCIe Port14	
Lane21	SATA3 Port2	PCIe Port15	
Lane22	SATA3 Port3	PCIe Port16	M.2 SSD (SATA)

HM175		Grolsch
USB20	USB2 Port1	USB 3.0 (MB) (S/C)
USB20	USB2 Port2	USB 3.0 (MB)
USB20	USB2 Port3	USB 3.0 (I/O)
USB20	USB2 Port4	USB3 (Type C)
USB20	USB2 Port5	USB3 (Type C)
USB20	USB2 Port6	
USB20	USB2 Port7	M.2 BT
USB20	USB2 Port8	Touch panel
USB20	USB2 Port9	CCD (WEBCAM)
USB20	USB2 Port10	CR(USB)
USB20	USB2 Port11	Finger Print
USB20	USB2 Port12	
USB20	USB2 Port13	
USB20	USB2 Port14	

NOTE:
Lynx Point: USB2[0:13]
Sunrise Point PCH-H: USB2[1:14]

U2000A

DMI

5 DMI_TXP0	N27	DMI_RXP0
5 DMI_TXN0	L27	DMI_RXN0
5 DMI_RXP0	B27	DMI_TXP0
5 DMI_RXN0	C27	DMI_TXN0
5 DMI_TXP1	G24	DMI_RXP1
5 DMI_TXN1	E24	DMI_RXN1
5 DMI_RXP1	A28	DMI_TXP1
5 DMI_RXN1	B28	DMI_TXN1
5 DMI_TXP2	E26	DMI_RXP2
5 DMI_TXN2	G27	DMI_RXN2
5 DMI_RXP2	C29	DMI_TXP2
5 DMI_RXN2	B29	DMI_TXN2
5 DMI_TXP3	K29	DMI_RXP3
5 DMI_TXN3	L29	DMI_RXN3
5 DMI_RXP3	A30	DMI_TXP3
5 DMI_RXN3	B30	DMI_TXN3

USB2.0

USB2P_1	AG7	1PD 14-24KOHM	USB_PP1	52
USB2N_1	AF5	1PD 14-24KOHM	USB_PN1	52
USB2P_2	AD7	1PD 14-24KOHM	USB_PP2	52
USB2N_2	AD5	1PD 14-24KOHM	USB_PN2	52
USB2P_3	AG10	1PD 14-24KOHM	USB_PP3	64
USB2N_3	AG8	1PD 14-24KOHM	USB_PN3	64
USB2P_4	AE2	1PD 14-24KOHM	USB_PP4	42
USB2N_4	AE1	1PD 14-24KOHM	USB_PN4	42
USB2P_5	AC3	1PD 14-24KOHM	USB_PP5	42
USB2N_5	AC2	1PD 14-24KOHM	USB_PN5	42
USB2P_6	AF3	1PD 14-24KOHM		
USB2N_6	AF2	1PD 14-24KOHM		
USB2P_7	AB2	1PD 14-24KOHM	USB_PP7_BT	53
USB2N_7	AB3	1PD 14-24KOHM	USB_PN7_BT	53
USB2P_8	AL7	1PD 14-24KOHM	USB_PP8_TP	45
USB2N_8	AL8	1PD 14-24KOHM	USB_PN8_TP	45
USB2P_9	AA2	1PD 14-24KOHM	USB_PP9_CCD	45
USB2N_9	AA1	1PD 14-24KOHM	USB_PN9_CCD	45
USB2P_10	AJ7	1PD 14-24KOHM	USB_PP10_CR	64
USB2N_10	AJ8	1PD 14-24KOHM	USB_PN10_CR	64
USB2P_11	W3	1PD 14-24KOHM	USB_PP11_FP	69
USB2N_11	W2	1PD 14-24KOHM	USB_PN11_FP	69
USB2P_12	AD2	1PD 14-24KOHM		
USB2N_12	AD3	1PD 14-24KOHM		
USB2P_13	V1	1PD 14-24KOHM		
USB2N_13	V2	1PD 14-24KOHM		
USB2P_14	AJ13	1PD 14-24KOHM		
USB2N_14	AJ11	1PD 14-24KOHM		

USB3.0 on-board
USB3.0 IO-board
TYPE-C On-board
M.2 BT
Touch Panel
WEBCAM
CARD READER
Finger Printer

PCIE/USB/SATA

B16	PCIE1_TXP/USB3_7_TXP	
A16	PCIE1_TXN/USB3_7_TXN	
G15	PCIE1_RXP/USB3_7_RXP	
H15	PCIE1_RXN/USB3_7_RXN	
C19	PCIE2_TXP/USB3_8_TXP	
B19	PCIE2_TXN/USB3_8_TXN	
G17	PCIE2_RXP/USB3_8_RXP	
E17	PCIE2_RXN/USB3_8_RXN	
C20	PCIE3_TXP/USB3_9_TXP	
B20	PCIE3_TXN/USB3_9_TXN	
K17	PCIE3_RXP/USB3_9_RXP	
L17	PCIE3_RXN/USB3_9_RXN	
A21	PCIE4_TXP/USB3_10_TXP	
B21	PCIE4_TXN/USB3_10_TXN	
G19	PCIE4_RXP/USB3_10_RXP	
E20	PCIE4_RXN/USB3_10_RXN	
C22	PCIE5_TXP	
D22	PCIE5_TXN	
L19	PCIE5_RXP	
K19	PCIE5_RXN	
A23	PCIE6_TXP	
B22	PCIE6_TXN	
E22	PCIE6_RXP	
G22	PCIE6_RXN	
B23	PCIE7_TXP	
C23	PCIE7_TXN	
K22	PCIE7_RXP	
L22	PCIE7_RXN	
B24	PCIE8_TXP	
C24	PCIE8_TXN	
L24	PCIE8_RXP	
K24	PCIE8_RXN	
B31	PCIE9_TXP/SATA0A_TXP	
C31	PCIE9_TXN/SATA0A_TXN	
H31	PCIE9_RXP/SATA0A_RXP	
G31	PCIE9_RXN/SATA0A_RXN	
B32	PCIE10_TXP/SATA1A_TXP	
C32	PCIE10_TXN/SATA1A_TXN	
E29	PCIE10_RXP/SATA1A_RXP	
G29	PCIE10_RXN/SATA1A_RXN	
B33	PCIE11_TXP	
C33	PCIE11_TXN	
K31	PCIE11_RXP	
L31	PCIE11_RXN	
A35	PCIE12_TXP	
B35	PCIE12_TXN	
H33	PCIE12_RXP	
G33	PCIE12_RXN	

USB3.0

USB3_1_TXP	B11			
USB3_1_TXN	C11			
USB3_1_RXP	A7			
USB3_1_RXN	B7			
USB3_2_TXP	A12		USB3_TXP2	52
USB3_2_TXN	B12		USB3_TXN2	52
USB3_2_RXP	B8		USB3_RXP2	52
USB3_2_RXN	C8		USB3_RXN2	52
USB3_3_TXP	D13		USB3_TXP3	52
USB3_3_TXN	C13		USB3_TXN3	52
USB3_3_RXP	A9		USB3_RXP3	52
USB3_3_RXN	B10		USB3_RXN3	52
USB3_4_TXP	B13		USB3_TXP4	64
USB3_4_TXN	A14		USB3_TXN4	64
USB3_4_RXP	G11		USB3_RXP4	64
USB3_4_RXN	E11		USB3_RXN4	64
USB3_5_TXP	C14		USB3_TXP5	41
USB3_5_TXN	B14		USB3_TXN5	41
USB3_5_RXP	H13		USB3_RXP5	41
USB3_5_RXN	G13		USB3_RXN5	41
USB3_6_TXP	C15			
USB3_6_TXN	B15			
USB3_6_RXP	K13			
USB3_6_RXN	K15			

USB3.0(S/C) on-board
USB3.0 On-board
USB3.0 IO-board
USB3.0 TYPE-C

USB2_ID
USB2_VBUSSENSE

AG2 IWPU USB2_ID
AD10 USB2_VBUSSENSE

R2000 1KOhm 1%
SR2001 0Ohm @/SP
GND
GND

WIGIG

53 PCIE_TXP_WIGIG	C2022	2	1	0.1UF/6.3V	PCIE_TXP_WIGIG_C
53 PCIE_TXN_WIGIG	C2023	2	1	0.1UF/6.3V	PCIE_TXN_WIGIG_C
53 PCIE_RXP_WIGIG					
53 PCIE_RXN_WIGIG					

M.2 WLAN

53 PCIE_TXP_WLAN	C2020	2	1	0.1UF/6.3V	PCIE_TXP_WLAN_C
53 PCIE_TXN_WLAN	C2021	2	1	0.1UF/6.3V	PCIE_TXN_WLAN_C
53 PCIE_RXP_WLAN					
53 PCIE_RXN_WLAN					

SATA

51 PCIE_TXP9	
51 PCIE_TXN9	
51 PCIE_RXP9	
51 PCIE_RXN9	

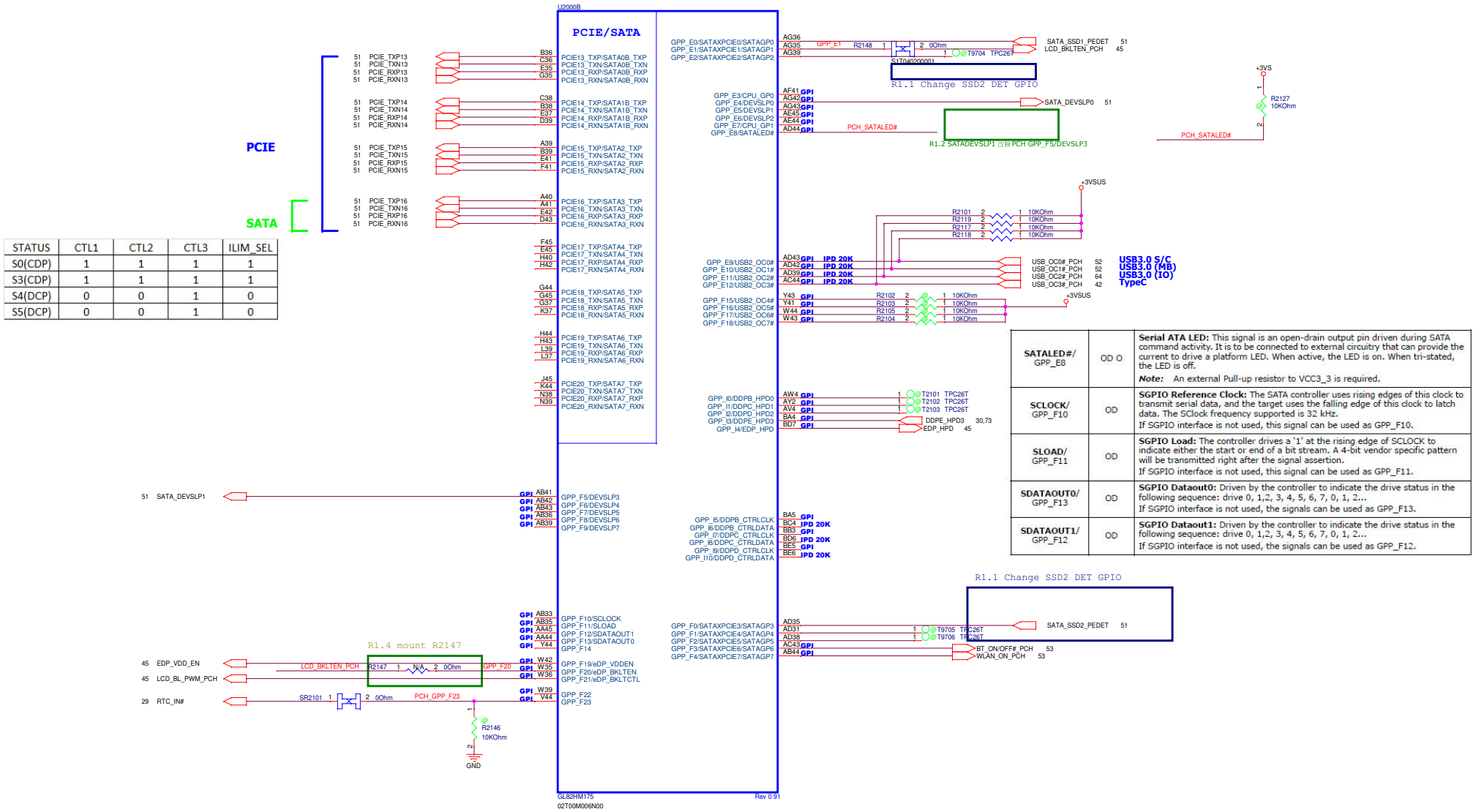
PCIE

51 PCIE_TXP10	
51 PCIE_TXN10	
51 PCIE_RXP10	
51 PCIE_RXN10	
51 PCIE_TXP11	
51 PCIE_TXN11	
51 PCIE_RXP11	
51 PCIE_RXN11	
51 PCIE_TXP12	
51 PCIE_TXN12	
51 PCIE_RXP12	
51 PCIE_RXN12	

GL82HM175 Rev 0.91
02T00M006N00

PEGATRON Title: PCH_DMI/PCIE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: James Liao
Size C | Project Name GS5FA | Rev 1.0
Date: Monday, December 10, 2018 | Sheet 20 of 98

21 PCH(2) PCIE/SATA



STATUS	CTL1	CTL2	CTL3	ILIM_SEL
S0(CDP)	1	1	1	1
S3(CDP)	1	1	1	1
S4(DCP)	0	0	1	0
S5(DCP)	0	0	1	0

SATALED#/ GPP_E8	OD O	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. ***Note:*** An external Pull-up resistor to VCC3_3 is required.
SCLOCK/ GPP_F10	OD	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SClock frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as GPP_F10.
SLOAD/ GPP_F11	OD	**SGPIO Load:** The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as GPP_F11.
SDATAOUT0/ GPP_F13	OD	**SGPIO Dataout0:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1,2, 3, 4, 5, 6, 7, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPP_F13.
SDATAOUT1/ GPP_F12	OD	**SGPIO Dataout1:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1,2, 3, 4, 5, 6, 7, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPP_F12.

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Title: PCH_SATA/PCIE

Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Tuesday, December 11, 2018 Sheet 21 of 98

22 PCH(3) ESPI/SPI/FAN/HOST

+3VS +3VSUS — +3VS 6,21,23,24,26,30,31,32,36,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92 ; +3VSUS 6,21,23,24,26,28,29,30,31,36,51,53,62,64,81,88,92

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

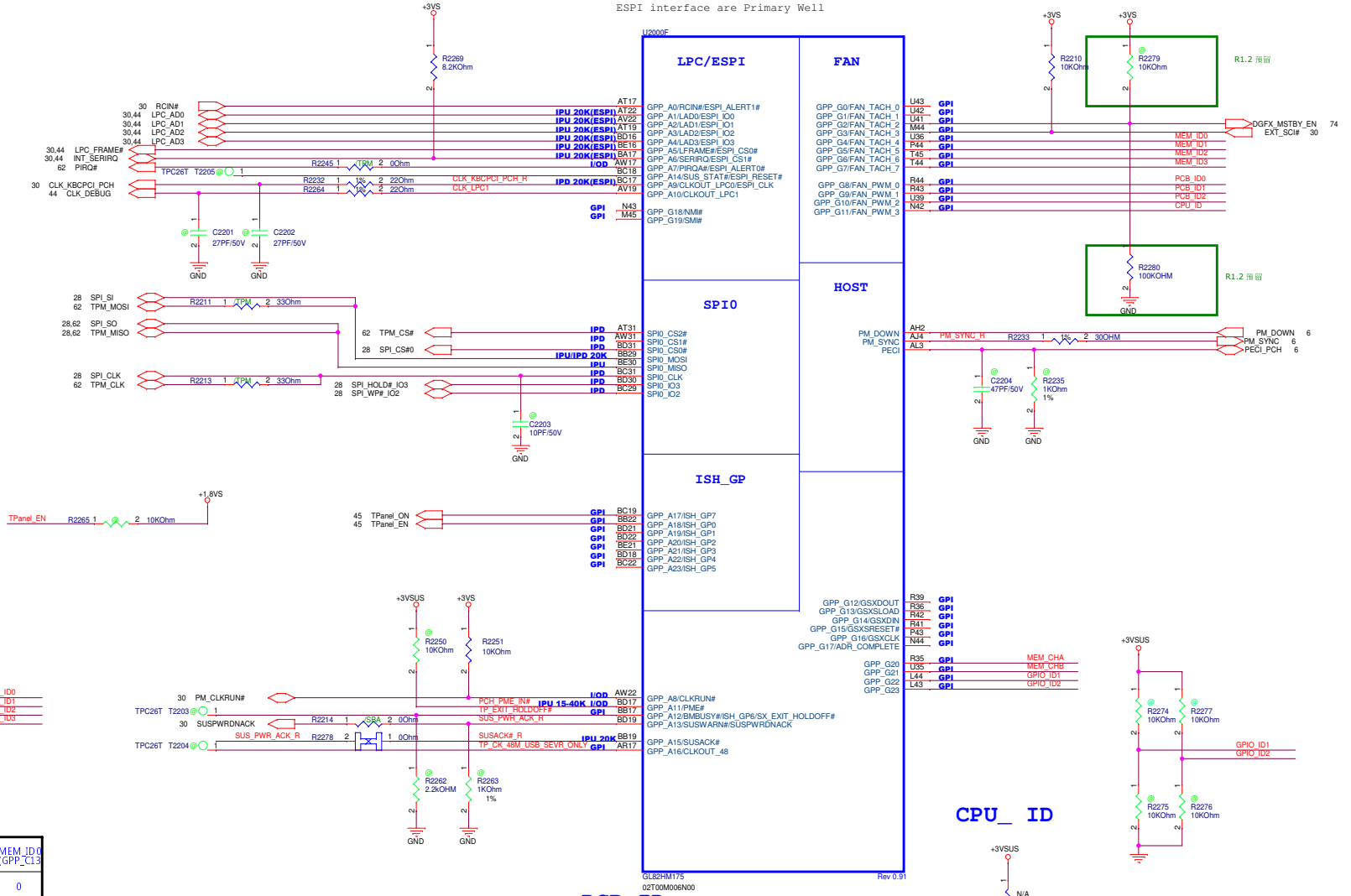
NOTE:
CLKOUT_LPC[0:1] are 24MHz(TBD) with Rs=22ohm
ESPI_CLK is xxHz with Rs=15ohm

NOTE:
Check PCA spec SIO_SMI# to GPIO or SMI#?

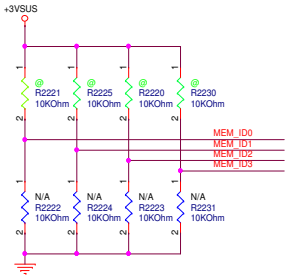
NOTE:
TBD; Check ISH GPIO[0:7]
PU/PD and power rail

NOTE:
ESPI_ALERT[0:1]# & ESPI_CS1# are Server Only
ESPI interface are Primary Well

NOTE:
Check PCA spec for specific implementation

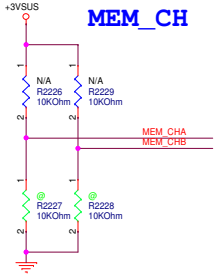


MEM ID



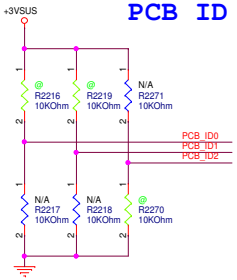
	MEM_ID3 (GPP_C23)	MEM_ID2 (GPP_C14)	MEM_ID1 (GPP_C13)	MEM_ID0 (GPP_C13)
MICRON 2666 MT40A512M16LY-075:E SDP 0315-02DW0PB	0	0	0	0
HYNIX 2400 H5AN8G6NAFR-UHC SDP 0315-01W60PB	0	0	0	1
HYNIX 2666 H5AN8G6NCJR-VKC SDP 0315-02GJ0PB	0	0	1	0
MICRON 2400 MT40A1G16WBU-083E:B DDP 0315-01YC0PB	0	0	1	1
HYNIX 2400 H5ANAG6NAMR-UHC DDP 0315-02640PB	0	1	0	0
MICRON 2666 MT40A1G16KNR-075:E DDP 0315-02FY0PB	0	1	0	1
	0	1	1	0

MEM_CH ID



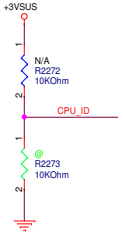
	CHA	CHB
Disable	0	
Enable	1	
Disable		0
Enable		1

PCB ID



	PCB_ID2 (GPP_C23)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0	0
R11	0	0	1
R12	0	1	0
R13	0	1	1
R14	1	0	0
R20	1	0	1

CPU_ ID



	CPU_ID
VPOR	0
Non-VPRO	1

PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>

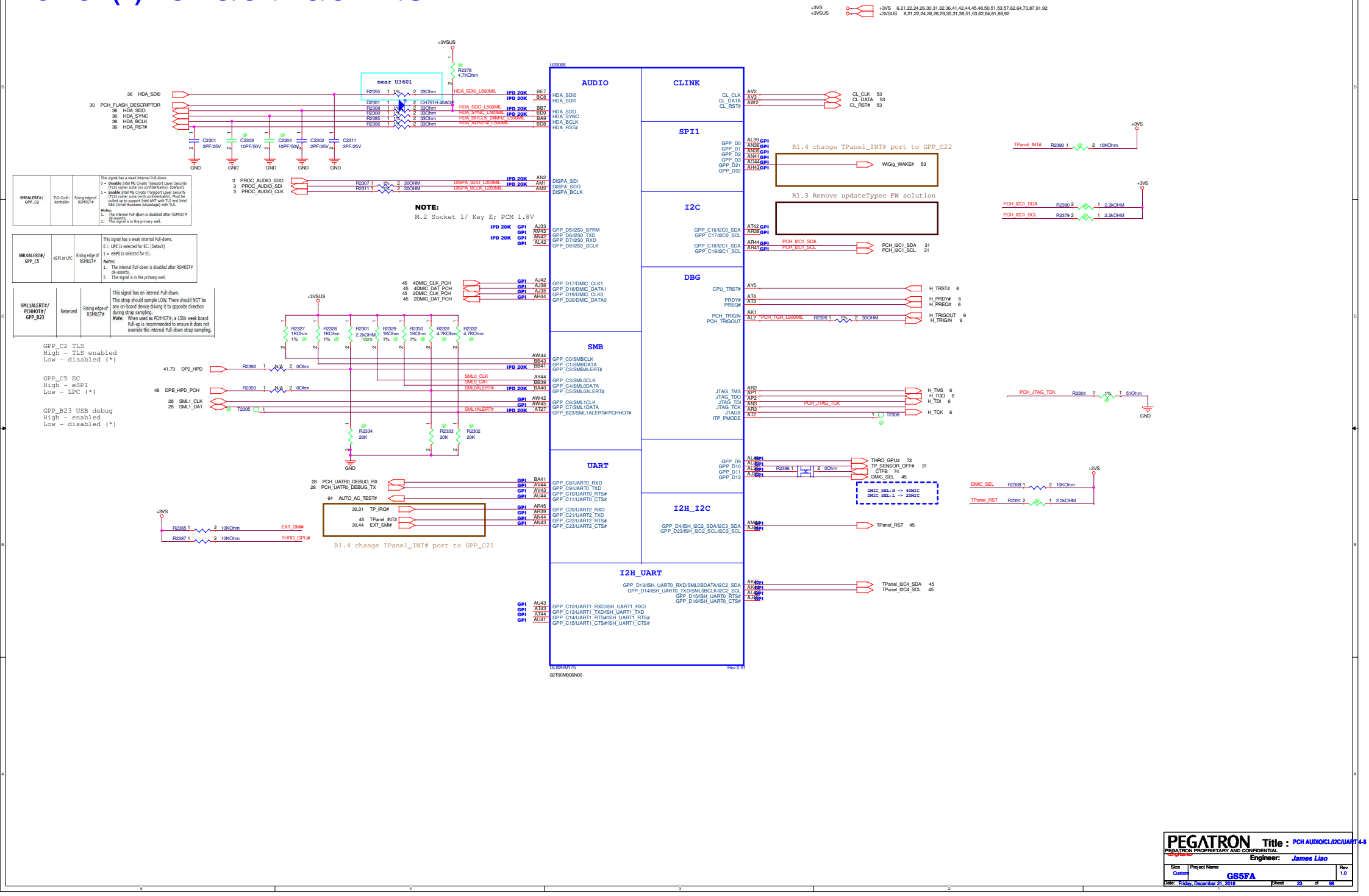
Title : PCH_ESPI/SPI/FAN/HOST

Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Friday, December 21, 2018 Sheet 22 of 98

23 PCH(4) AUDIO/CL/I2C/UART/SMB



PEGATRON Title : PCH AUDIO/CL/I2C/UART 4-8
PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>
Engineer: James Liao
Size Custom | Project Name GS5FA | Rev 1.0
Date: Friday, December 21, 2018 | Sheet 23 of 68

24 PCH(5) GPSI/POWER MANAGE

NOTE:
GSPI0_MOSI/GPP_B18

0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:
GPP_B22/GSPI1_MOSI

Offset 3410h:Bit 10
0: SPI
1: LPC

Check power rail

+3VS 6,21,22,23,26,30,31,32,36,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92
+3VSUS 6,21,22,23,26,28,29,30,31,36,51,53,62,64,81,88,92
+VCC_RTC 26,29,60
+1.0V 6,9,57,80,91
+1.2V 6,9,15,16,17,19,48,57,83
+V3.3_DGFX_GPU 57,72,73,74,75,91

GSPI
ISH_I2C

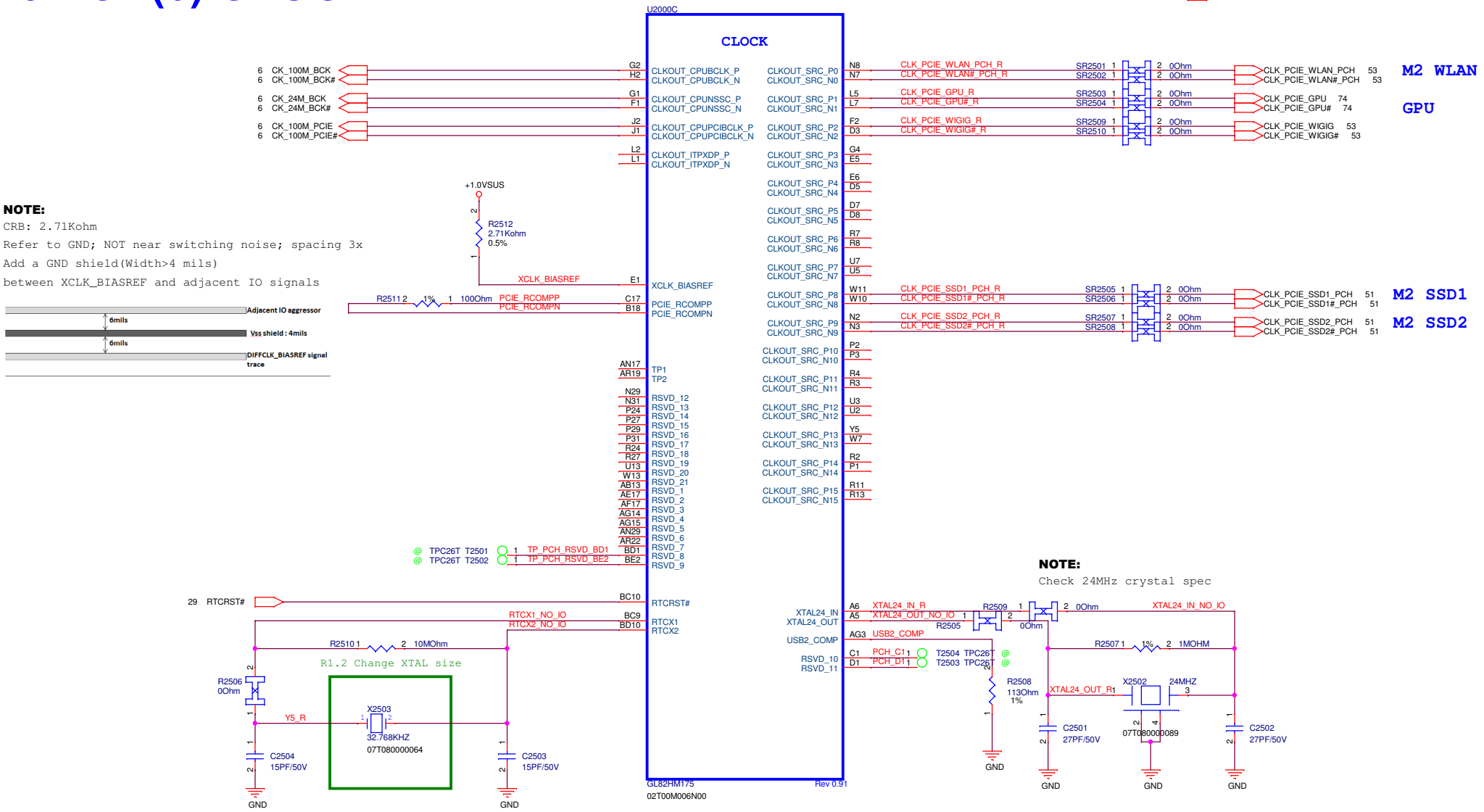
NOTE:
SML[2:4] are
Server Only

GL82HM175
02T00M006N00
Rev 0.91

Title	PCH_SML
Engineer	James Liao
Size	Custom
Project Name	GS5FA
Rev	1.0
Date	Monday, December 10, 2018
Sheet	24 of 98

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
001-HWG RD

25 PCH(6) CLOCK



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Title : PCH_CLOCK
Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Friday, December 28, 2018 Sheet 25 of 98

26 PCH(7) POWER

NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

+3VS +3VSUS — +3VS 6,21,22,23,24,30,31,32,36,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92 / +3VSUS 6,21,22,23,24,28,29,30,31,36,51,53,62,64,81,88,92

+3VA +VCC_RTC +1.0VSUS — +3VA 30,31,36,57,67,81,88,93 / +VCC_RTC 24,29,60 / +1.0VSUS 25,82

U2000G

PRIMARY
VCCPRIM_1p0_15
VCCPRIM_1p0_11
VCCPRIM_1p0_12
VCCPRIM_1p0_13
VCCPRIM_1p0_14
VCCPRIM_1p0_4
VCCPRIM_1p0_8
VCCPRIM_1p0_17
VCCPRIM_1p0_16
VCCPRIM_1p0_2
VCCPRIM_1p0_1
VCCPRIM_1p0_3
VCCPRIM_1p0_7
VCCPRIM_1p0_10
VCCPRIM_1p0_9
VCCPRIM_1p0_6
VCCPRIM_1p0_5

CLOCK
VCCCLK5_1
VCCCLK5_2
VCCCLK1
VCCCLK3
VCCCLK4
VCCCLK2_2
VCCCLK2_1

MPHY
VCCMPHY_1p0_1
VCCMPHY_1p0_2
VCCMPHY_1p0_3
VCCMPHY_1p0_4
VCCMPHY_1p0_5
VCCAMPHYPLL_1p0_1
VCCAMPHYPLL_1p0_2
VCCMIPIPLL_1P0_2
VCCMIPIPLL_1P0_1

VCCGPIO
VCCGPPA
VCCGPPBCH_1
VCCGPPBCH_2
VCCGPPEF_1
VCCGPPEF_2
VCCGPPG
VCCGPPD_3
VCCGPPD_1
VCCGPPD_4
VCCGPPD_2

SPI
VCCSPI_1
VCCSPI_3
VCCSPI_2

PRIMARY
VCCPRIM_3p3_2
VCCPRIM_3p3_3
VCCPRIM_3p3_4
VCCPRIM_3p3_1
VCCRTCPRIM_3p3
VCCATS
VCCDSW_3p3_1
VCCDSW_3p3_2
VCCHDA
VCCRTC

VCCAPLLEBB_1p0
VCCUSB2PLL_1p0_1
VCCUSB2PLL_1p0_2
VCCHDAPLL_1P0
DCPDSW_1p0
DCPRTC

GL82HM175
02T00M006N00
Rev 0.91

+1.0VSUS — @ JP2602 2MM_OPEN_5MIL — @ JP2601 1MM_OPEN_M1M2 — +1V_PRIM_W12MIL — Icc(max):6.01A
C2616 22UF/6.3V, C2604 22UF/6.3V, C2640 0.1UF/6.3V
near AJ20

+1.0VSUS — @/SP SR2605 0Ohm — +V1P0A_VCCF24_W15MIL — Icc(max):0.007A
C2619 22UF/6.3V, @C2620 22UF/6.3V, C2608 1UF/6.3V
near K2/K3
Icc(max):0.332A

+1.0VSUS — Icc(max):0.08A
C2641 0.1UF/6.3V, C2607 22UF/6.3V, C2614 1UF/6.3V
near U21

+1.0VSUS — @/SP SR2607 0Ohm — +V1P0A_VCCAMPHYPLL_W25MIL — Icc(max):0.11A
C2628 22UF/6.3V, @C2625 22UF/6.3V, C2617 1UF/6.3V
near A43

+VCCAPLLEBB_1p0 — R2613 0Ohm — Icc(max):0.03A
+V1P0A_VCCAPLL_W15MIL — Icc(max):0.045A
C2638 0.1UF/6.3V

+1.0VSUS — B2603 75Ohm 09T010000096 — +VCCAPLLEBB_1p0
C2636 2PF/25V, C2637 2PF/25V
near V28

+1V_DCPDSW — DCPRTC
C2602 1UF/6.3V, C2623 0.1UF/6.3V
near BJ29, near BA26

+3VSUS — R2611 0Ohm — B2601 75Ohm — +DVDDIO_AUDIO_W10MIL
C2629 2PF/25V, C2630 2PF/25V, C2642 0.1UF/6.3V
near BA15

+1.0VSUS — R2612 0Ohm — B2602 75Ohm — +V1P0A_VCCAPLL_W15MIL
C2632 2PF/25V, C2633 2PF/25V, C2634 22UF/6.3V, @C2635 22UF/6.3V, C2639 0.1UF/6.3V
near AJ5

+3VSUS — Icc(max):0.082A — R2610 @/SP
Icc(max):0.408A — @/SP SR2602 0Ohm — +3VSUS
C2626 0.1UF/6.3V, C2601 0.1UF/6.3V, C2603 0.1UF/6.3V, C2606 0.1UF/6.3V
near BA31, near BC42

NOTE:
Place 0.1uF near U3.BC42/ AJ41/ AD41 pins

NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

+3VSUS — Icc(max):0.078A — @/SP SR2604 0Ohm — +VCCPGPPCD_W15MIL

GPIO Group	Power Pins	Voltage
Primary Well Group A(GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B(GPP_B) Primary Well Group C(GPP_C) Primary Well Group H(GPP_H)	VCCPGPPBCH	1.8V or 3.3V
Primary Well Group D(GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E(GPP_E) Primary Well Group F(GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G(GPP_G)	VCCPGPPG	1.8V or 3.3V
Primary Well Group I(GPP_I)	VCCPRIM_3P3	3.3V
Deep Sleep Well Group(GPD)	VCCDSW_3P3	3.3V

+3VSUS +3VA — Icc(max):0.029A — R2604 0Ohm, R2601 0Ohm

NOTE:
1.8V SPI(with Quad IO) is expensive than 3.3V part

+3VSUS — Icc(max):0.117A — VCCPFUSE_W20MIL — @/SP SR2606 0Ohm
C2615 0.1UF/6.3V, C2605 22UF/6.3V, C2613 22UF/6.3V
near BD3

+3VSUS — Icc(max):0.001A
C2618 0.1UF/6.3V, C2610 1UF/6.3V
near BA20

NOTE:
Place 0.1uF near U3.AN5

+3VS — @/SP SR2603 0Ohm — Icc(max):0.007A
+3VSUS — Icc(max):0.195A — +VCCDSW_R2605 0Ohm
C2609 1UF/6.3V, C2612 1UF/6.3V
near AD13, near BA24

NOTE:
Place 1uF near U3.W15

+DVDDIO_AUDIO_W10MIL — Icc(max):0.06A
+VCCRTC_W8MIL — Icc(max):0.001A — SR2601 0Ohm @/SP — +VCC_RTC
C2624 0.1UF/6.3V, C2611 1UF/6.3V
near BA22

20160818 R12 Kai
mount circuit / unmount R2617

R2609 2.0Ohm — Q2601 PJA3411 — +3VSUS — +VCCDSW
R2607 100KOHM, Q2602 BC856BS, R2608 100KOHM

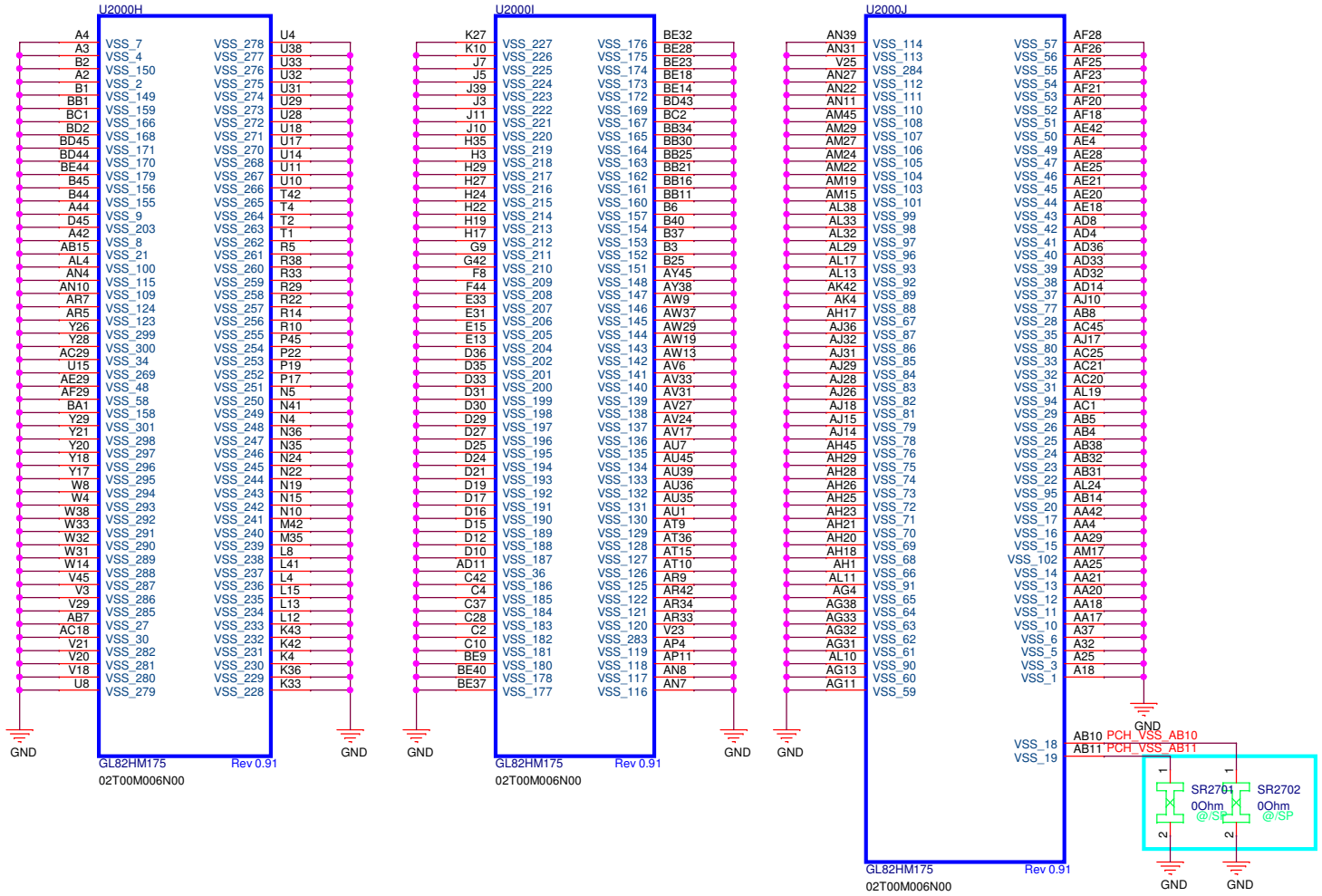
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title :
BGT-HW1 Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 26 of 98

27 PCH(8) VSS



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH_VSS

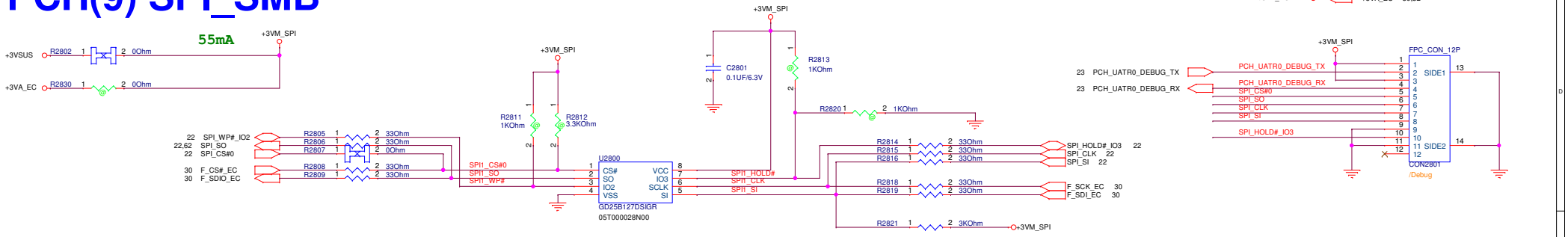
BG1-HW1

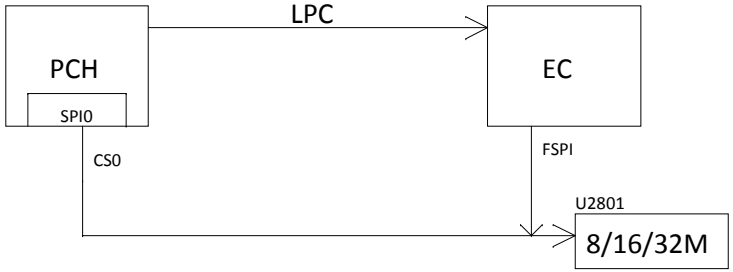
Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 27 of 98

28 PCH(9) SPI_SMB

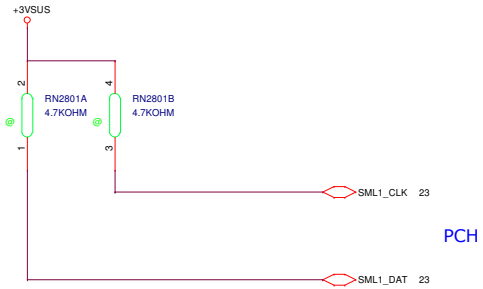




PCH SMBus

EC

GPU



PCH

PEGATRON Title : PCH(9)_SPI_SMB

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: James Liao

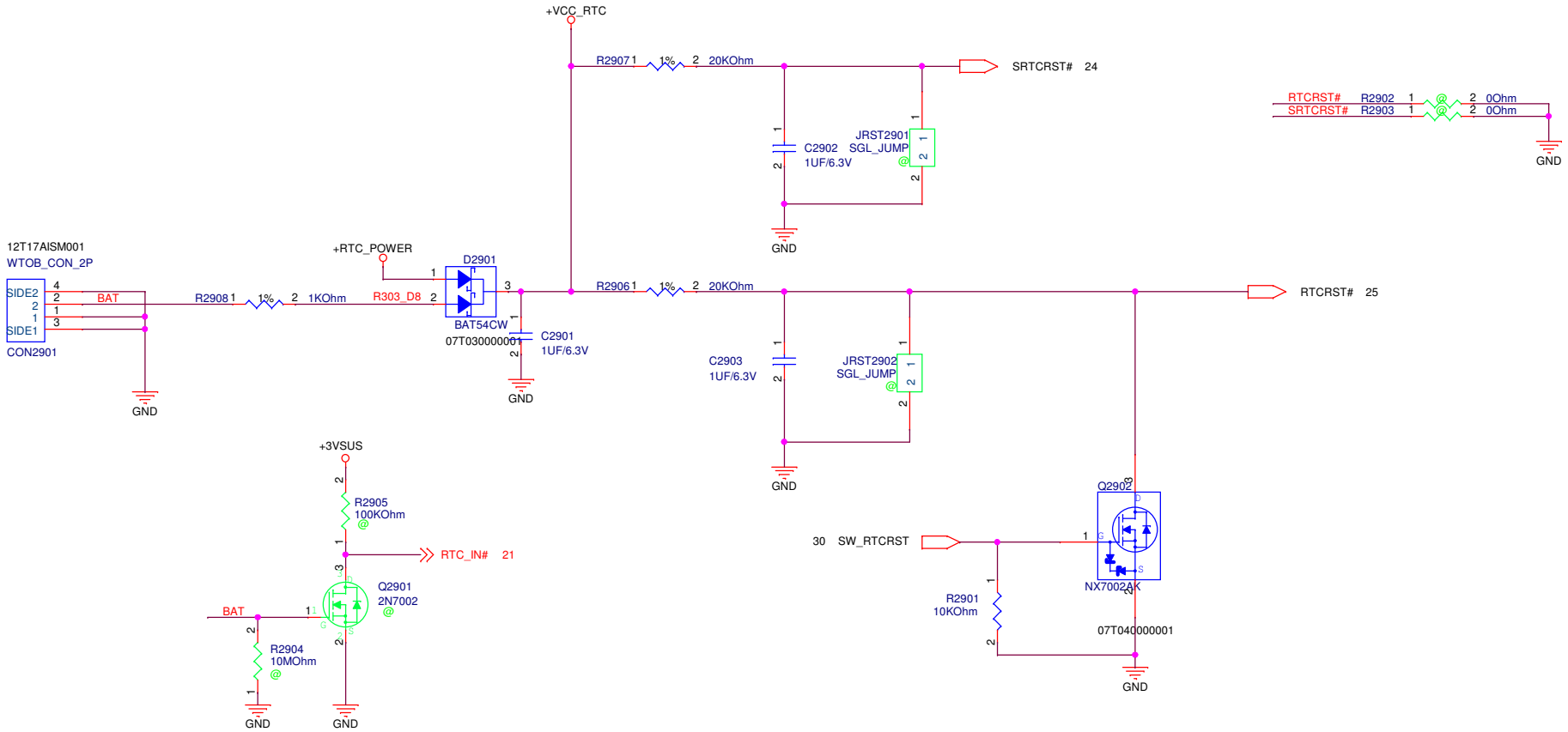
Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 28 of 98

29 RTC

+VCC_RTC
+RTC_POWER
+3VSUS

+VCC_RTC 24,26,60
+RTC_POWER 81
+3VSUS 6,21,22,23,24,26,28,30,31,36,51,53,62,64,81,88,92



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :

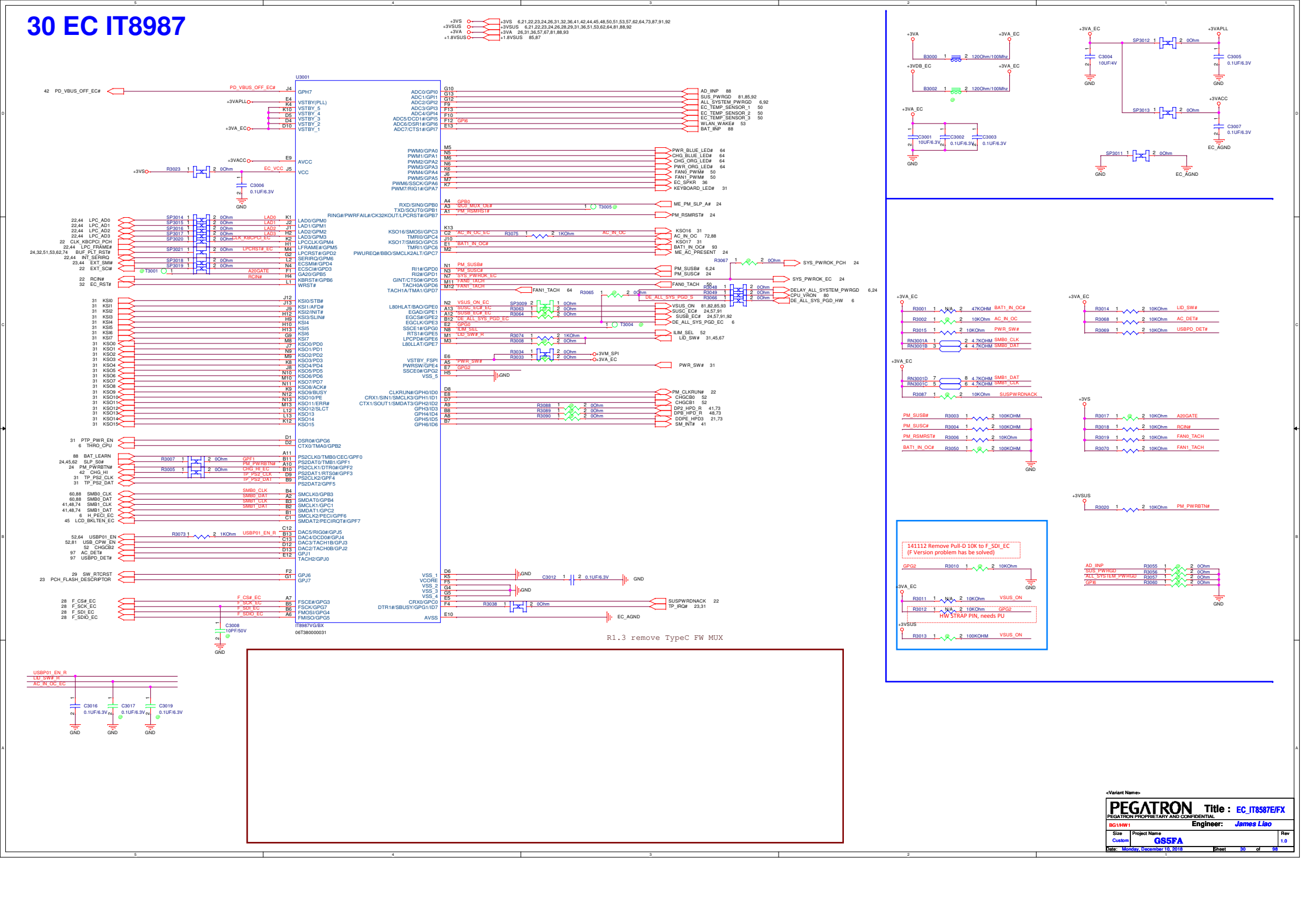
BG1-HW1

Engineer: James Liao

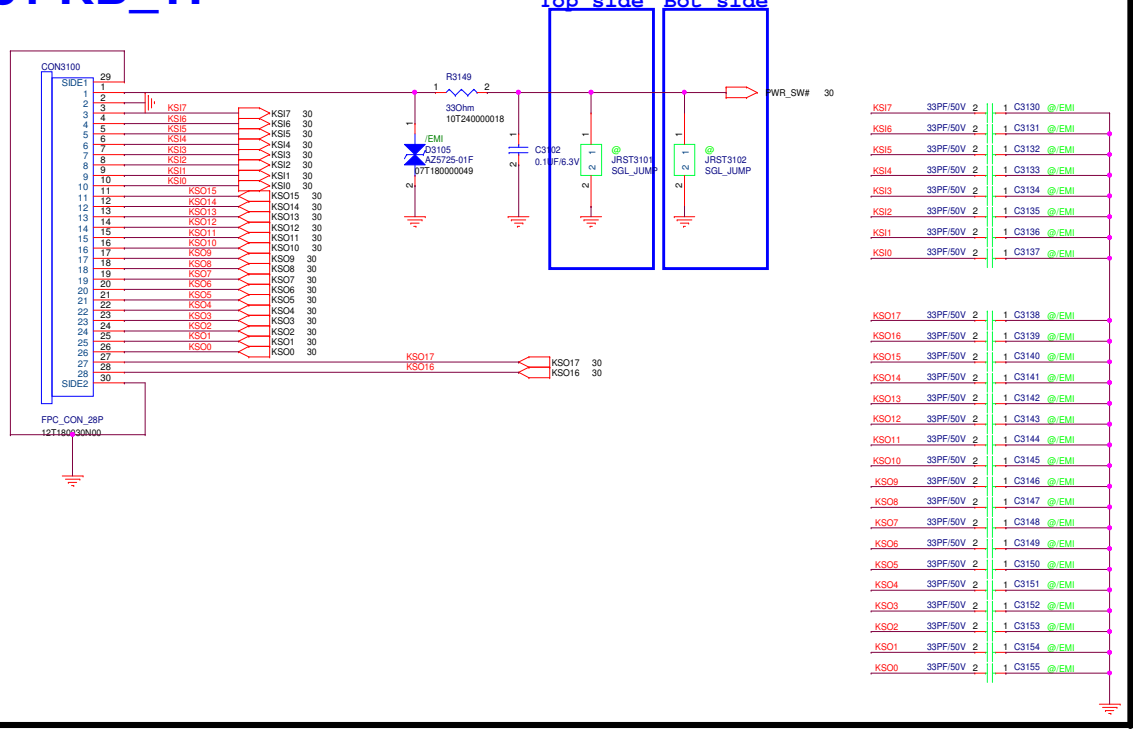
Size	Project Name	Rev
B	GS5FA	1.0

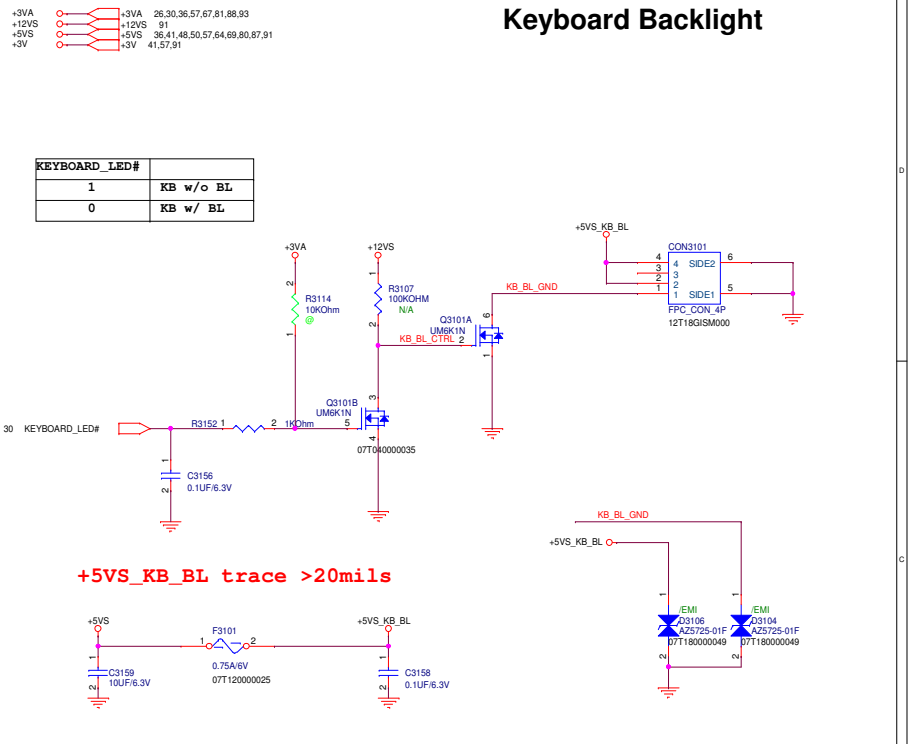
Date: Monday, December 10, 2018 Sheet 29 of 98

30 EC IT8987

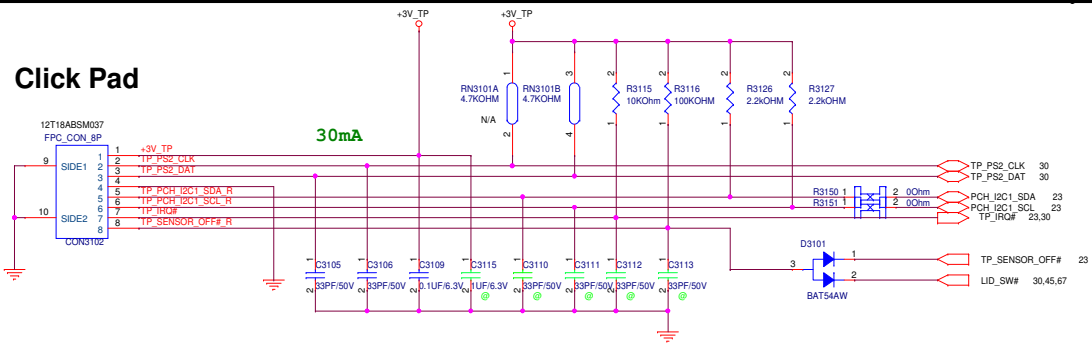

+3VS 6,21,22,23,24,26,31,32,36,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92
+3VSUS 6,21,22,23,24,26,28,29,31,36,51,53,62,64,81,88,92
+3VA 26,31,36,57,67,81,88,93
+1.8VSUS 85,87
U3001
IT8987VG/BX
067380000031
R1.3 remove TypeC FW MUX
141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)
HW STRAP PIN, needs PU
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EC_IT8587E/FX
Engineer: James Liao
BG1/HW1
Size Custom
Project Name GS5FA
Rev 1.0
Date: Monday, December 10, 2018
Sheet 30 of 98

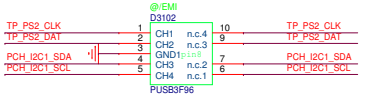
31 KB_TP

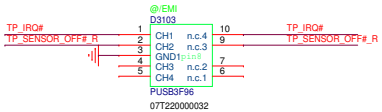


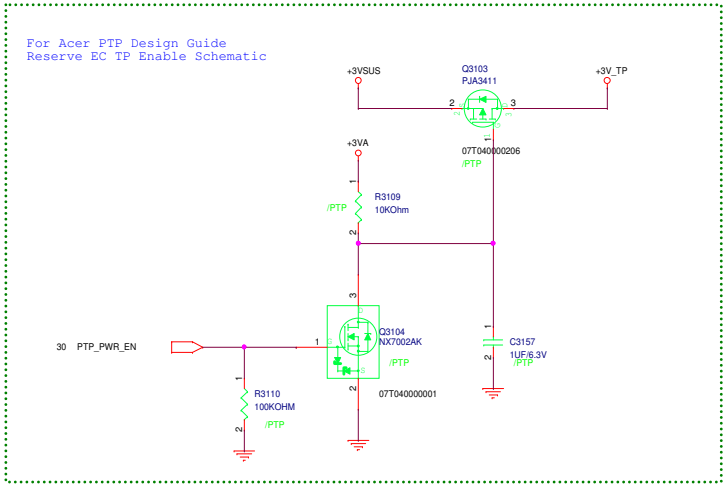


Click Pad



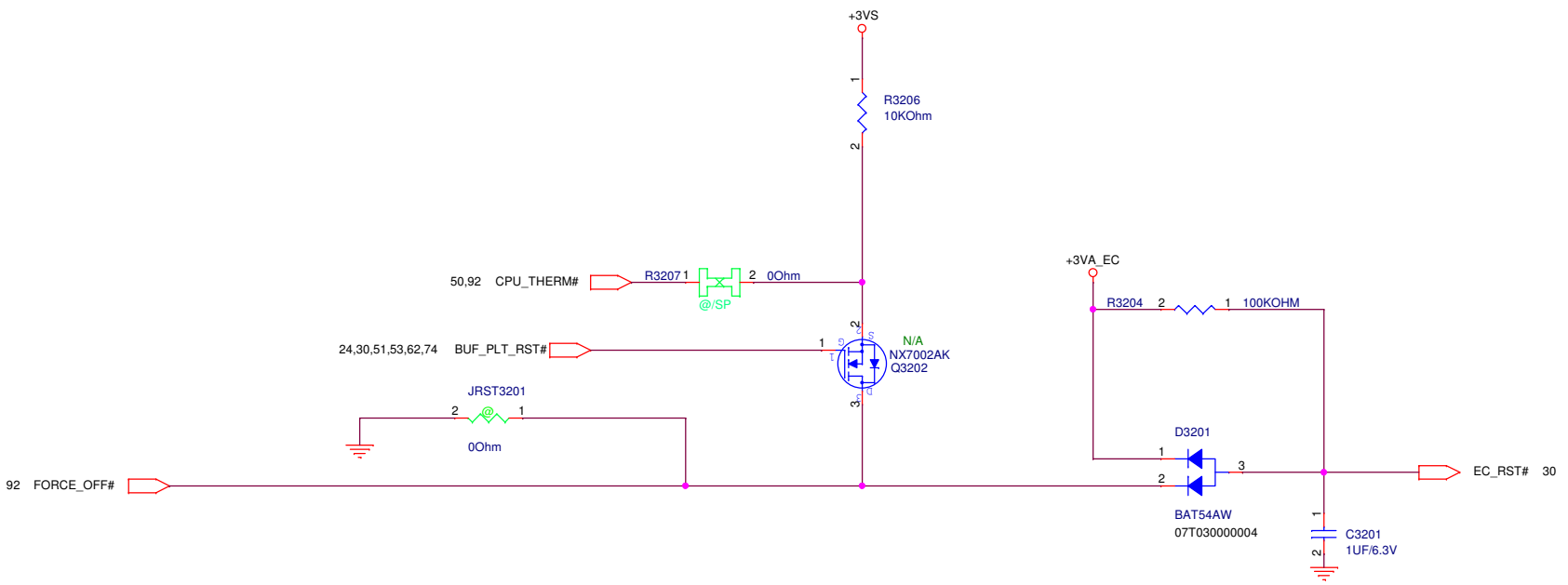






PEGATRON	Title : KB_TP
BG1/HW1	Engineer: James Liao
Size: C	Project Name: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 31 of 98

32 RST_Reset Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1/HW1

Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 32 of 98

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RTC

~~BG1-HW1~~

Engineer: *James Liao*

Size	Project Name	Rev
A	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 33 of 98

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	34 of 98

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	35 of 98

36 Audio Codec ALC256

+5VS +3VS +1.8VS +3VA

+5VS 31,41,48,50,57,64,69,80,87,91
+3VS 6,21,22,23,24,26,30,31,32,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92
+1.8VS 22,57,74,91
+3VA 26,30,31,57,67,81,88,93

Codec Power

+5VS Digital Analog +5VS_AUDIO

EMI D3602 AZ5725-01F 07T180000049

B3603 120Ohm/100Mhz

C3641 100PF/25V @EMI

C3642 100PF/25V @EMI

C3636 10UF/6.3V

Moat

GND AGND

In order to prevent the built-in LDO damaged from over-voltage on +5VS or Standby power line, we suggested using this Voltage suppressing device.

1.8V power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Please make sure that switching frequency operates at out- band(over 20Khz).

+1.8VS 50mA? +1.8VS_CDC_AVDD2

B3602 120Ohm/100Mhz

+1.8VS_AUDIO

R3620 0Ohm

+3VS +3VS_AUDIO

R3617 0Ohm

+3VA +3VA_CDC_STB

R3623 0Ohm

20171201 Raly
change resistor package size to 0402

Add this Filter to avoid other components/chips be influenced

+5VS L3601 600Ohm/100Mhz +5VS_PVDD_AVD

C3626 0.1UF/6.3V

C3629 10UF/6.3V

C3625 10UF/6.3V

C3624 0.1UF/6.3V

Close PIN 41

C3628 10UF/6.3V

C3627 0.1UF/6.3V

Close PIN 46

ALC256

Thermal pad = DGND

U3601A

+1.8VS_CDC_AVDD2 C3613 10UF/6.3V C3614 0.1UF/6.3V AGND Place close to Pin 40

C3615 10UF/6.3V +1.8VS_CDC_AVDD2

Analog Digital

+5VS_PVDD_AVD C3638 100PF/25V @EMI C3611 10UF/6.3V C3609 0.1UF/6.3V Place close to pin 41

C3608 10UF/6.3V C3610 0.1UF/6.3V Place close to pin 46

Powered by PVDD

Thermal PAD as PIN49: PVSS

C3617 1UF/6.3V

C3616 1UF/6.3V

+1.8VS_AUDIO C3622 10UF/6.3V

C3618 2.2uF/6.3V

C3619 10UF/6.3V

R3605 100KOhm

AGND

+5VS_AUDIO C3621 0.1UF/6.3V C3620 10UF/6.3V Place close to pin 26

AC_HP_R AC_HP_L

MIC2-VREFO-L MIC2-VREFO-R MIC2_VREFO

ANALOG_INL_C ANALOG_INR_C T3601 TPC26T T3602 TPC26T

LINE1_L LINE1_R +3VA_CDC_STB

C3623 10UF/6.3V

SLEEVE RING2

PC_BEEP

HP_JD#_C R3604 200KOhm HP_JD# HP_JD# 37

R3603 100KOhm +3VS_AUDIO

C3612 0.1UF/6.3V AGND

HDA_SPKR_LP HDA_SPKR_LN HDA_SPKR_RN HDA_SPKR_RP

PDB DMIC_DAT2

45 DMIC_DAT_P34

+3VS_AUDIO C3639 100PF/25V @EMI C3602 10UF/6.3V C3601 0.1UF/6.3V Place close to pin 1

45 DMIC_DAT_P12 DMIC_DAT1

HDA_SYNC HDA_SDI0 C3605 10UF/6.3V HDA_BCLK HDA_SDO

DMIC_CLK_R R3602 0Ohm DMIC_CLK 45

C3604 10PF/50V

+3VS_AUDIO C3606 0.1UF/6.3V C3607 10UF/6.3V C3640 100PF/25V @EMI Place close to Pin 9

U3601B PVSS_1 PVSS_2 PVSS_3 PVSS_4 PVSS_5 PVSS_6 PVSS_7 PVSS_8 PVSS_9 ALC256M-CG 02T0J0010N00

PC BEEP

PC_BEEP C3634 0.1UF/6.3V PCBEEP R3618 22KOhm R3622 0Ohm R3615 0Ohm

C3637 100PF/25V @

R3624 4.7KOhm

2 Path of SPKR

HDA_SPKR 24

EC_SPKR 30

MD3601 AZ5725-01F 07T180000049 EMI

MR3610 0Ohm MR3608 0Ohm MR3607 0Ohm MR3606 0Ohm

MC3630 100PF/25V MC3631 1000PF/25V MC3633 1000PF/25V

GND AGND

AMP De-Pop Control circuit

+3VS_AUDIO +3VSUS

R3611 100KOhm R3613 100KOhm

Q3602A UM6K1N Q3602B UM6K1N

PDB C3643 1UF/6.3V

24 OP_SD#

23 HDA_RST# R3612 100KOhm Q3601 LMBT3904LT1G

PEGATRON Title : Audio Codec ALC256

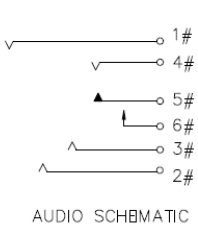
PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1-HW1 Engineer: James Liao

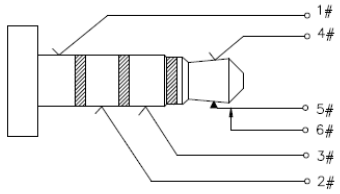
Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 36 of 98

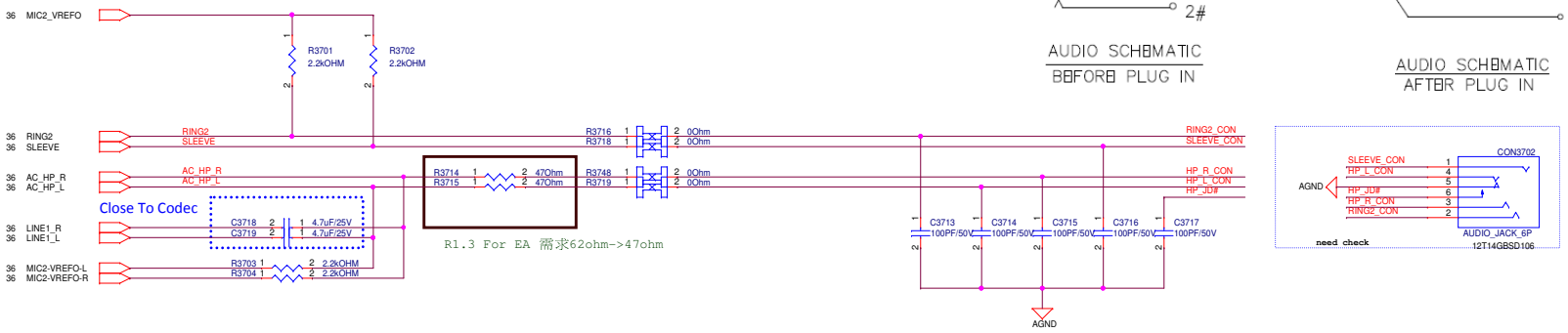
37 AUD_HP/DMIC/SPK

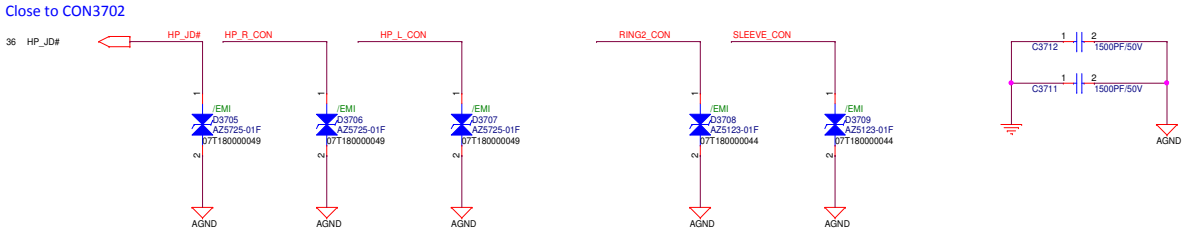


AUDIO SCHEMATIC
BEFORE PLUG IN

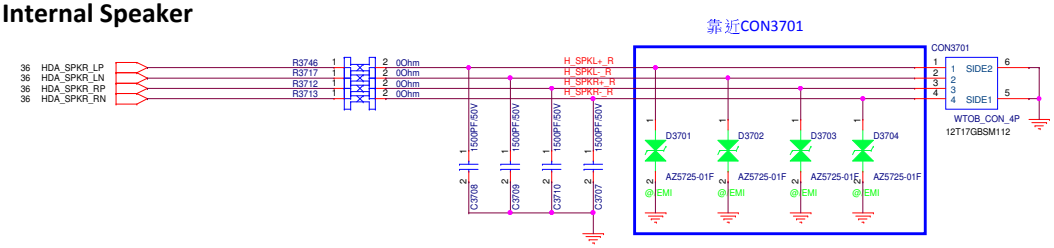


AUDIO SCHEMATIC
AFTER PLUG IN





Internal Speaker



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: AUD_HP/DMIC/SPK
3G1/HW1
Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Friday, December 21, 2018 Sheet 37 of 98

Title	<Title>
Size: A	Document Number: GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	38 of 98

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	39 of 98

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: DP Redriver PS8463

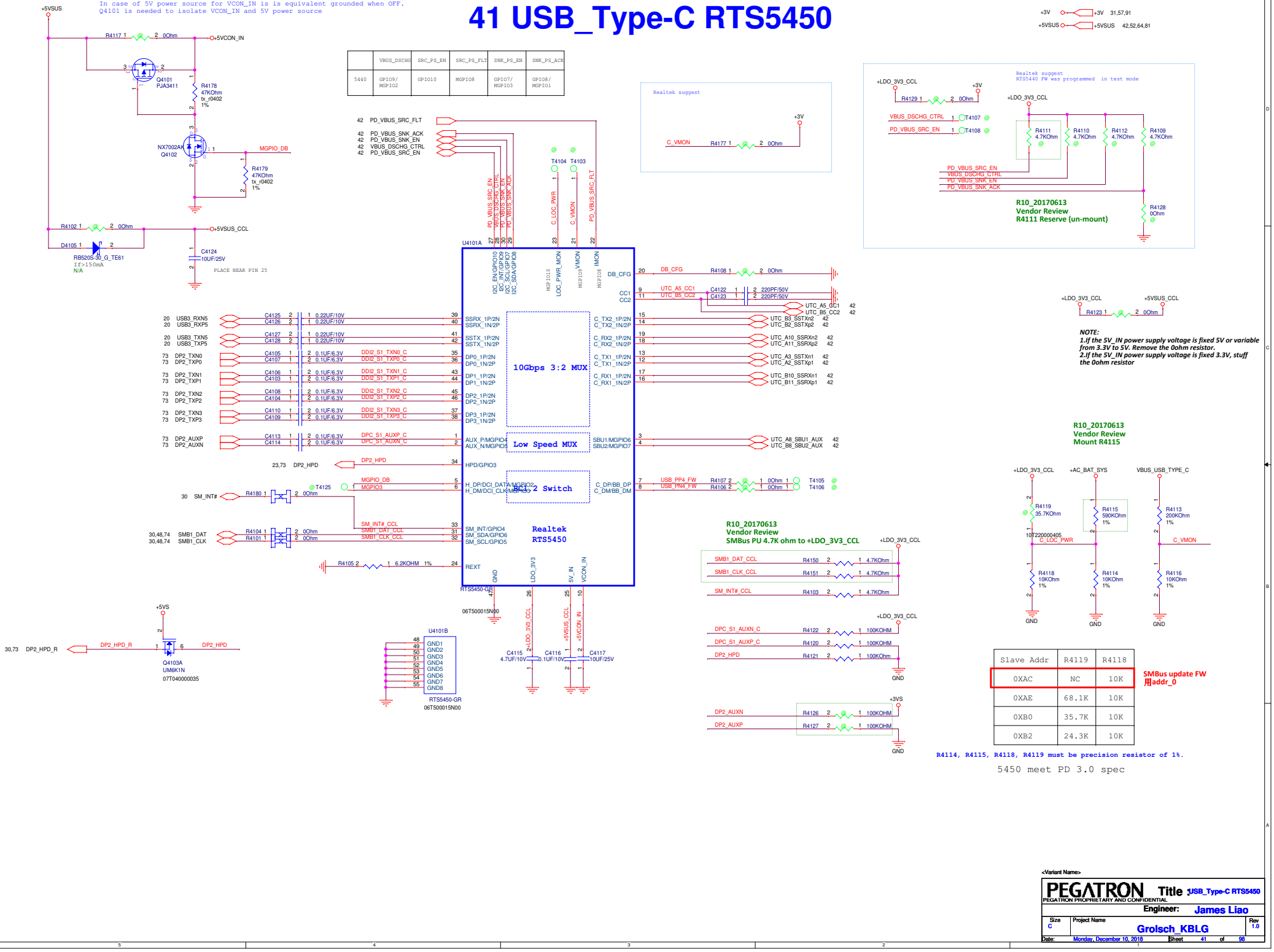
3G1-HW1

Engineer: James Liao

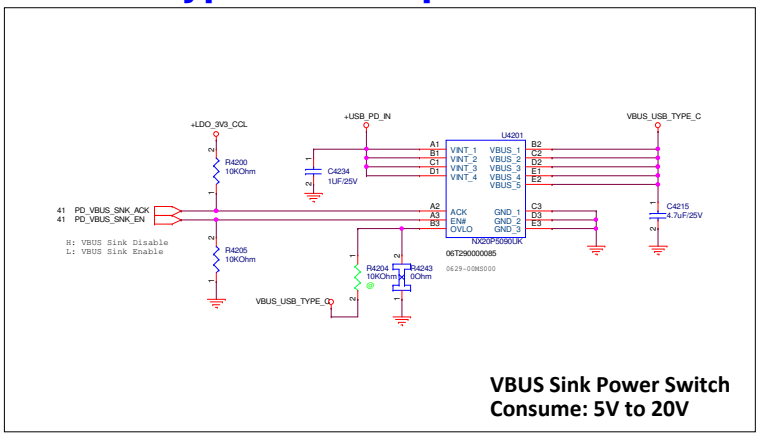
Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 40 of 98

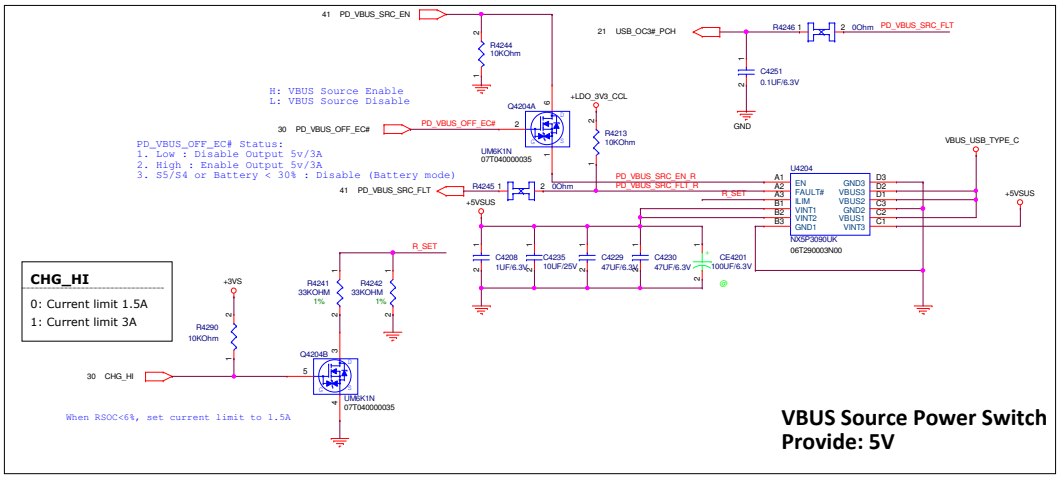
41 USB_Type-C RTS5450



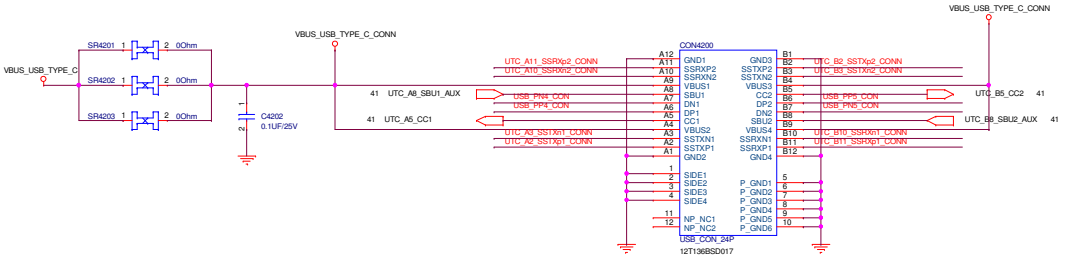
42 USB Type-C Receptacle



VBUS Sink Power Switch
Consume: 5V to 20V

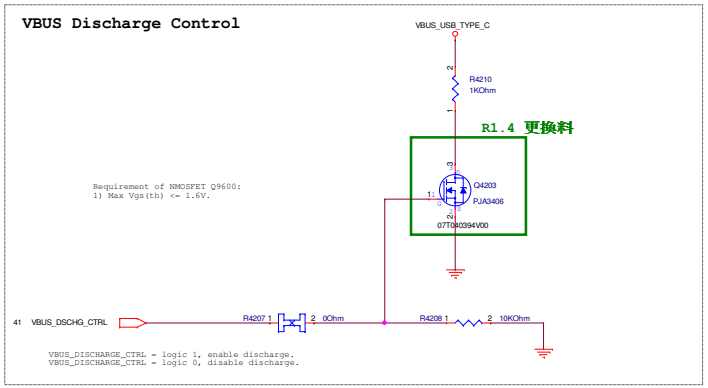


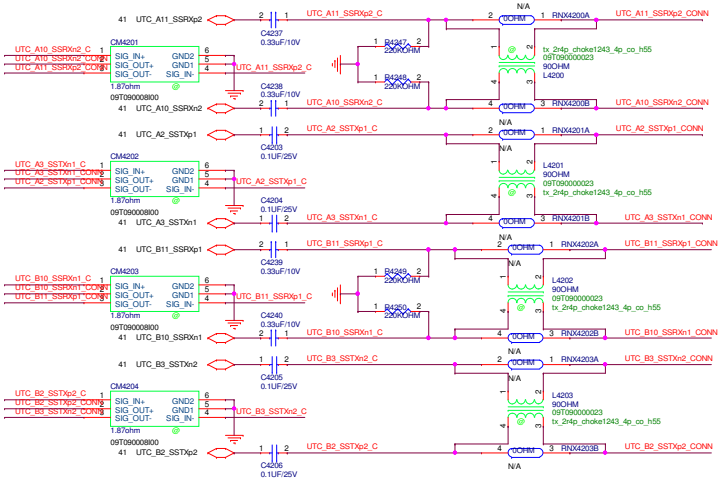
VBUS Source Power Switch
Provide: 5V

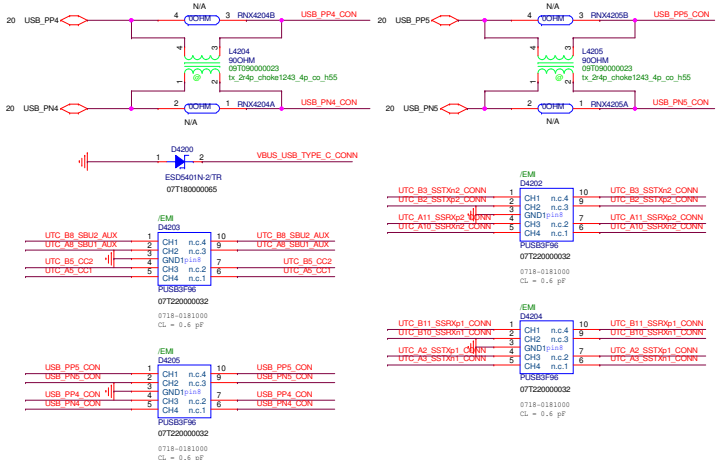


USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1







ESD

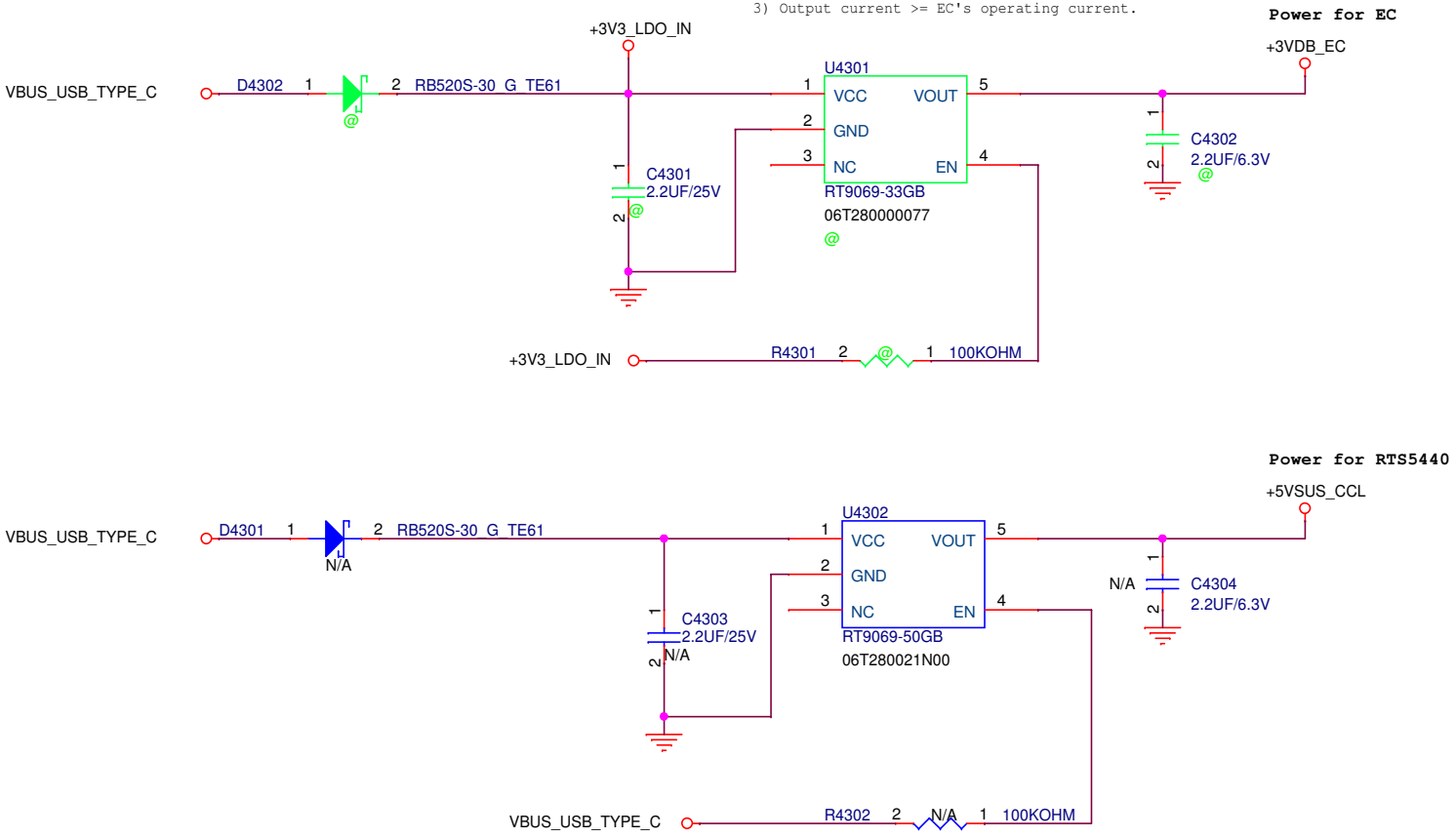
<Variant Name>
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: USB Type-C Receptacle
Engineer: James Liao
Size: Custom
Project Name: GS5FA
Rev: 1.0
Date: Monday, December 10, 2018
Sheet 42 of 58

43 Dead Battery

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C — VBUS_USB_TYPE_C 41,42
+AC_BAT_SYS — +AC_BAT_SYS 41,45,80,81,82,83,86,87,88,89,94
+3VDB_EC — +3VDB_EC 30
+5VSUS_CCL — +5VSUS_CCL 41



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery

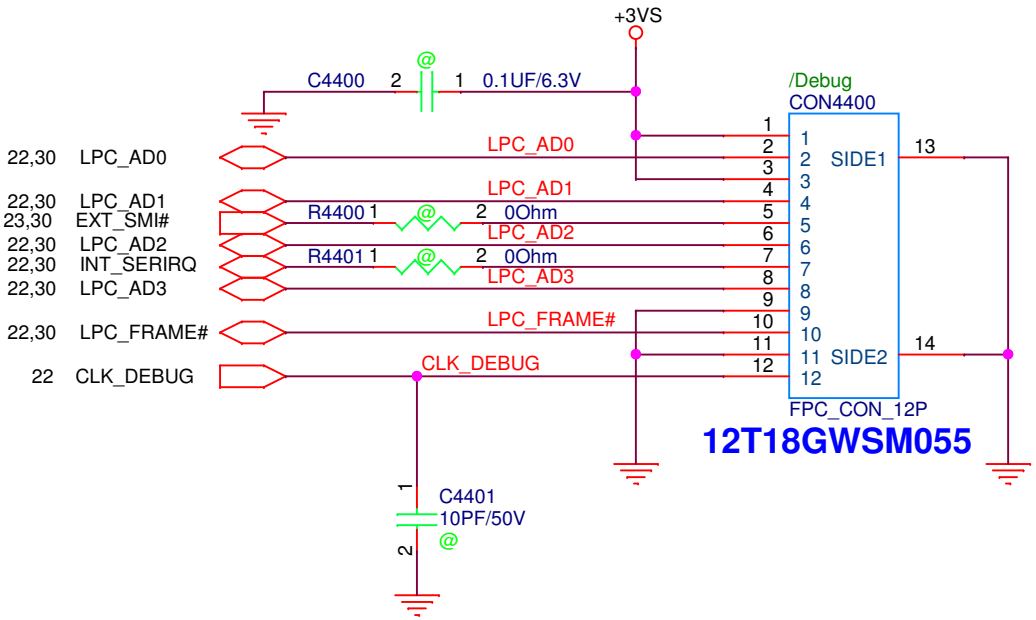
Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 43 of 98

44 DEBUG CONN.

+3VS +3VS 6,21,22,23,24,26,30,31,32,36,41,42,45,48,50,51,53,57,62,64,73,87,91



PEGATRON Title : DEBUG CONN.

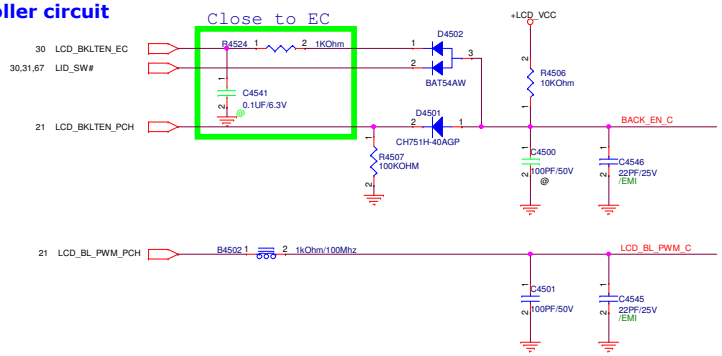
PEGATRON PROPRIETARY AND CONFIDENTIAL

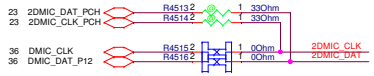
BG1/HW1 Engineer: *James Liao*

Size	Project Name	Rev
A	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 44 of 98

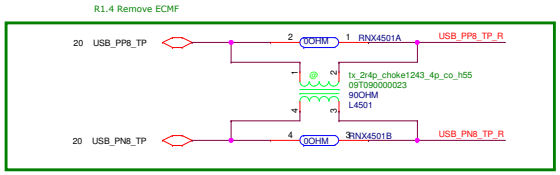
Controller circuit

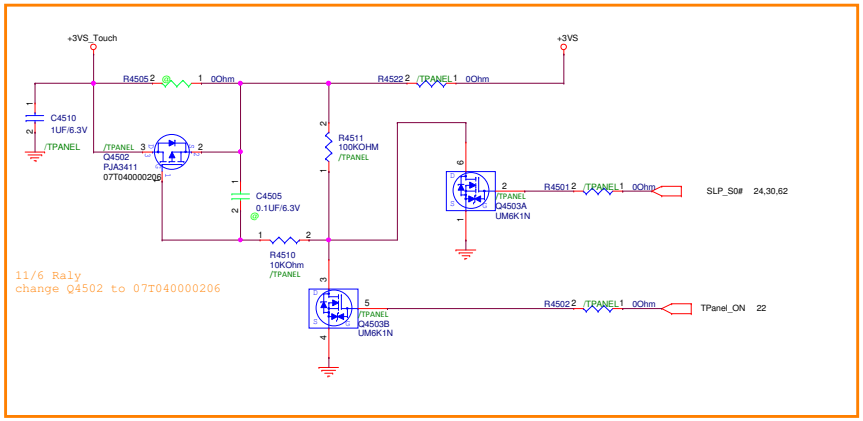




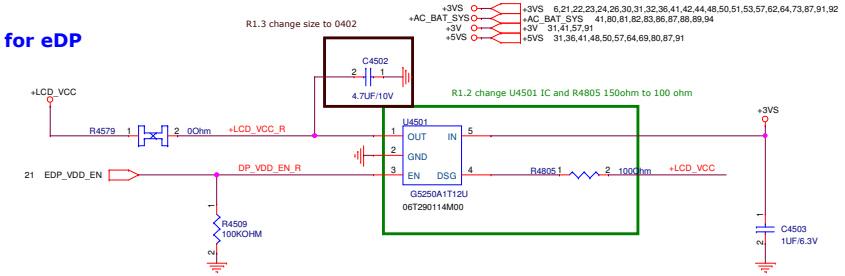
eDP HPD

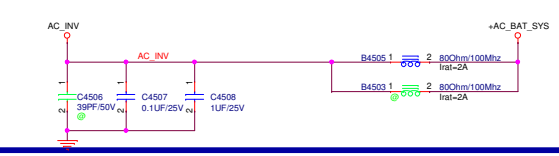
Touch panel

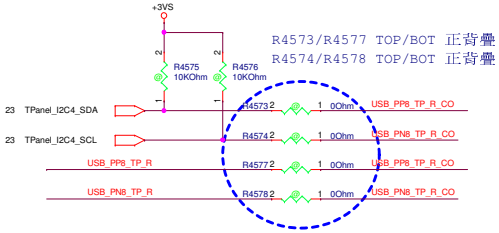


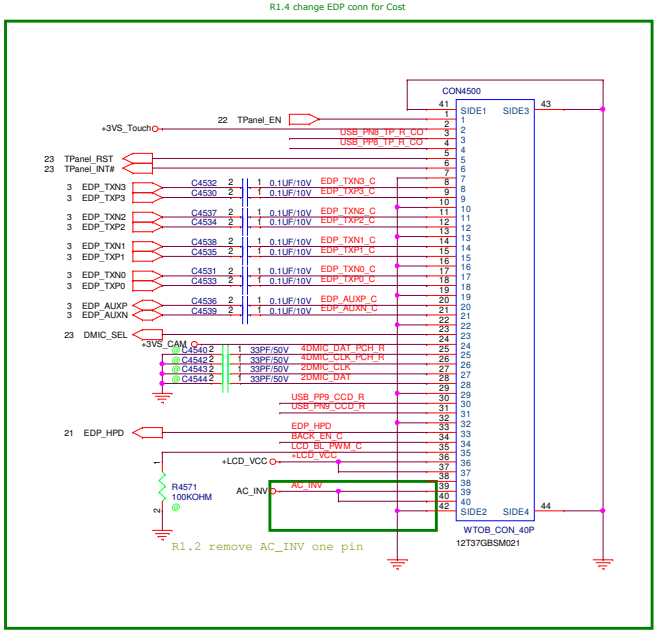


LCD_VCC for eDP

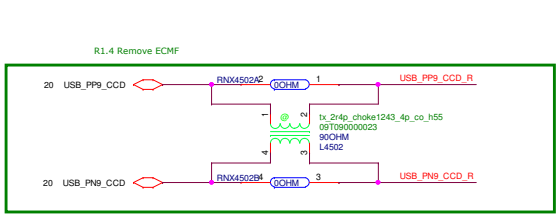


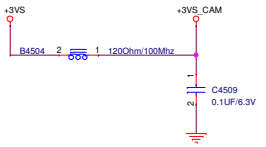






Camera





PEGATRON	Title : eDP Out		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW1	Engineer: James Liao		
Size: Custom	Project Name: GS5FA		Rev: 1.0
Date: Tuesday, December 11, 2018	Sheet 45 of 98		

Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 46 of 98

Title	<Title>
Size A	Document Number GS5FA
Rev	1.0
Date:	Monday, December 10, 2018
Sheet	47 of 98

48 HDMI 4K2K

[I2C_EN_PIN = 0] pin strap mode			
Net / Level	H	L	NC
PRE_SEL	Reserved	-2 dB	0 dB
EQ_SEL_A0	Fixed at 14 dB	Fixed at 7.5 dB	Adaptive EQ
SLEW_CTL	fastest data rate	5 ps slow	10 ps slow
HDMI_SEL#_TEST_A1	DVI	HDMI	N/A

[DP159 DDC on]
mount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
unmount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

[DP159 DDC snoop only] bypass I2C clock strength
unmount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
mount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

[I2C_EN_PIN = 1] I2C control mode
unmount R1320, mount R1319 / R1328 / R1329 / R1332 / R1333,

[I2C_EN_PIN = 0] pin strap mode
mount R1320, unmount R1319 / R1328 / R1329 / R1332 / R1333,
3-level setting (H / L / NC): PRE_SEL / EQ_SEL_A0 /SLEW_CTL
2-level setting (H / L): HDMI_SEL#_TEST_A1

R1.2 change power rail

For EMI request

50mA

325mA

Variant Name:	
PEGATRON CORPORATION PROPRIETARY AND CONFIDENTIAL	Title : HDMI-4K2K
EST-RW1	Engineer: James Liao
Size: D / Project Name: G65FA / Rev: 1.0	
Date: Wednesday, January 16, 2019	Sheet 48 of 98

<Variant Name>

PEGATRON

Title : eMMC

BG1/HW1

Engineer: James Liao

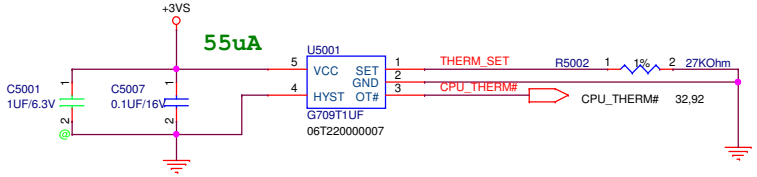
Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 49 of 98

50 Thermal_Fan

+5VS +5VS 31,36,41,48,57,64,69,80,87,91
+3VS +3VS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,51,53,57,62,64,73,87,91,92

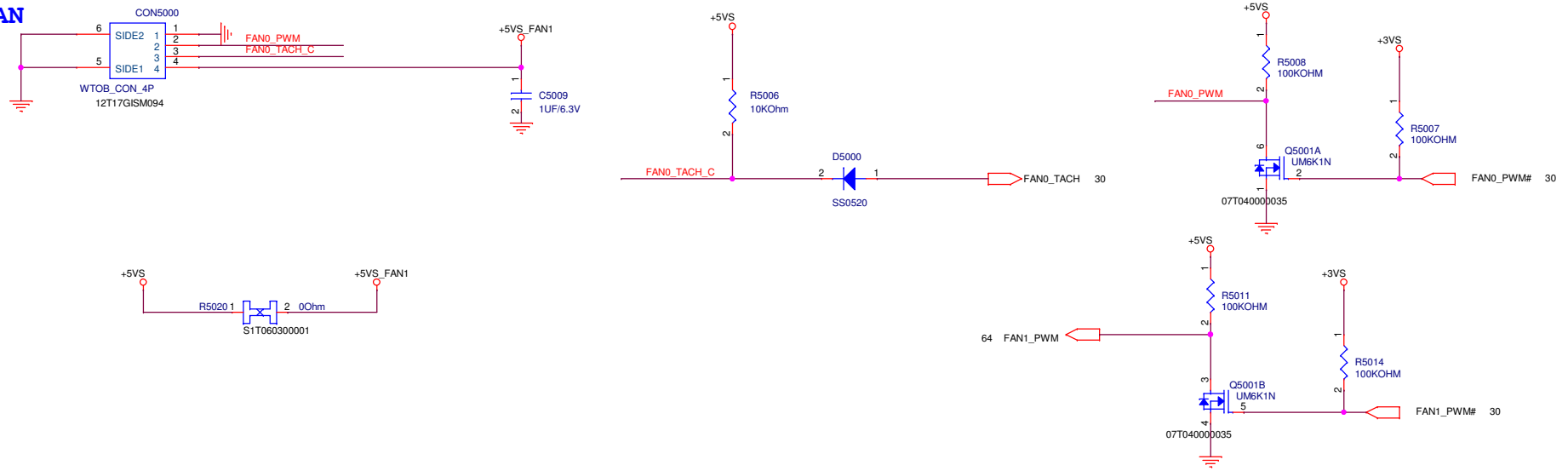
Thermal Sensor for package test



temp setting : 83 degree

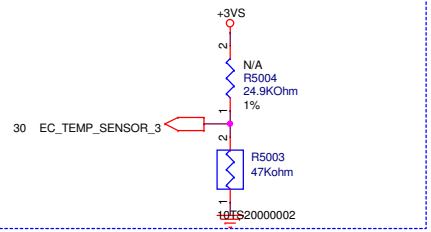
RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

FAN

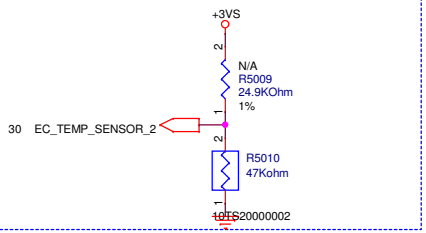


DPTF

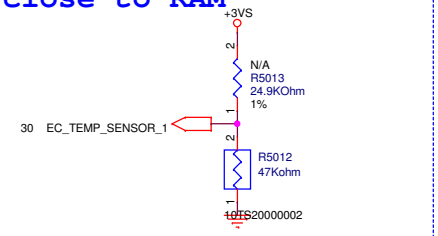
close to CPU VR



close to GPU VR



close to RAM



PEGATRON Title : Thermal_Fan
BG1/HW1 Engineer: James Liao

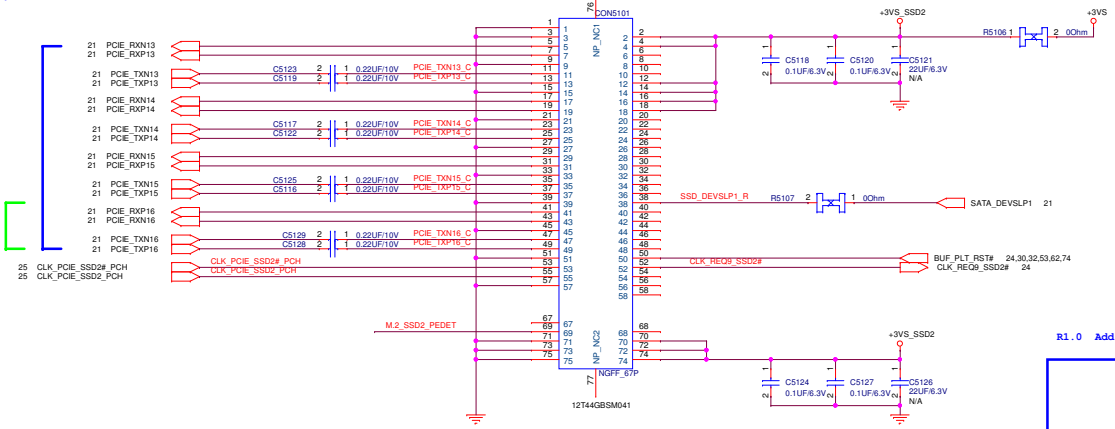
Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 50 of 98

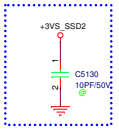
51 SATA/PCIE SSD

+3VS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,50,53,57,62,64,73,87,91,92
+5VS 31,36,41,48,50,57,64,69,80,87,91
+3VSUS 6,21,22,23,24,26,28,29,30,31,36,53,62,64,81,88,92

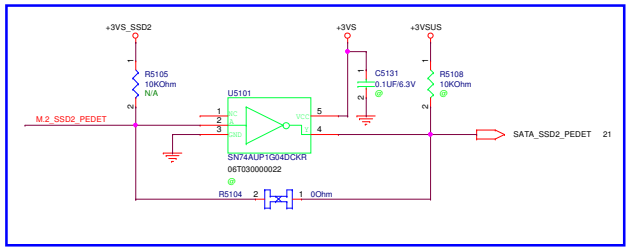
SATA / PCIe SSD 2



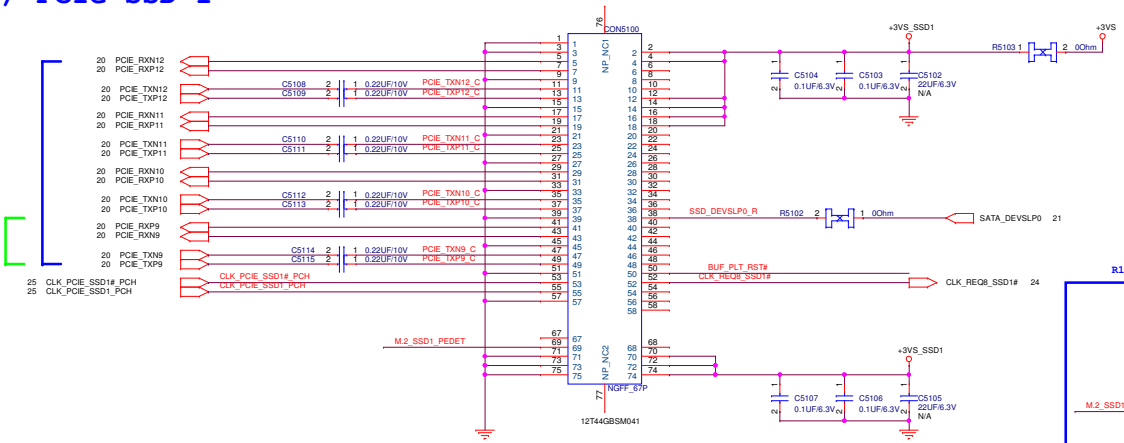
RF requirement



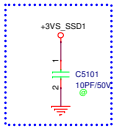
R1.0 Add SSD detect Follow PDG



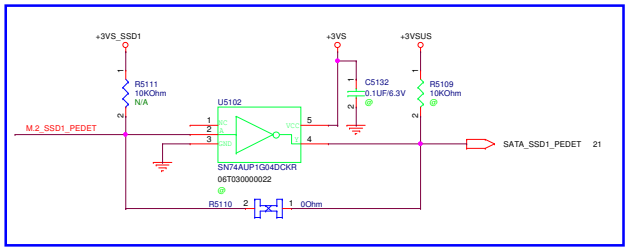
SATA / PCIe SSD 1



RF requirement



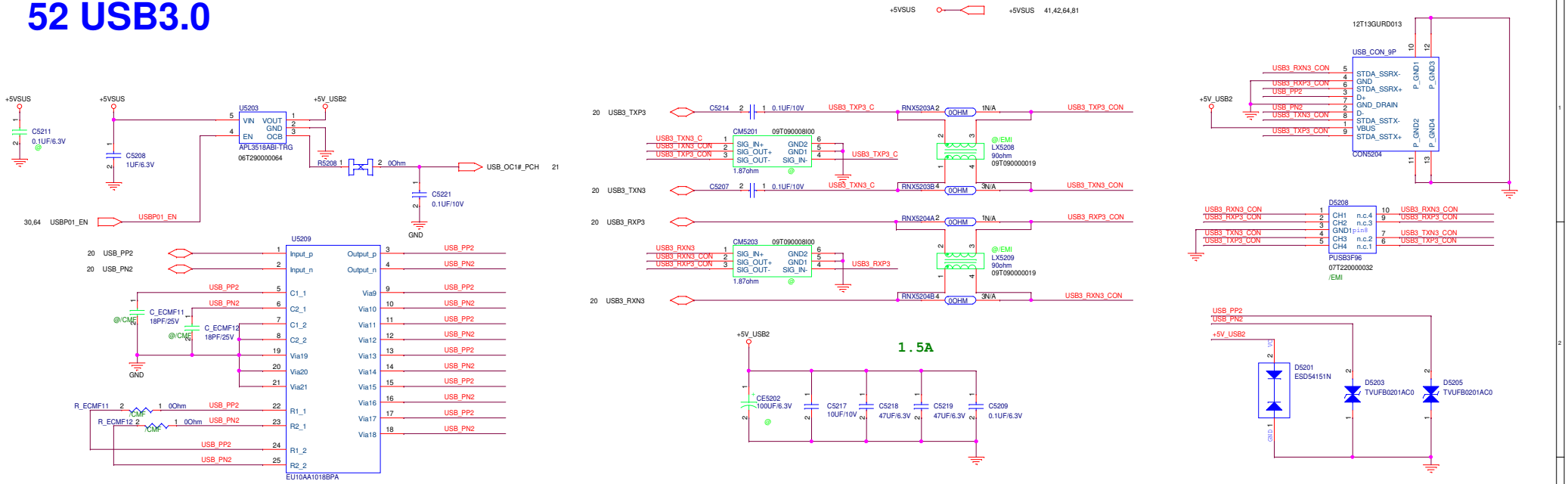
R1.0 Add SSD detect Follow PDG



PEGATRON PROPRIETARY AND CONFIDENTIAL

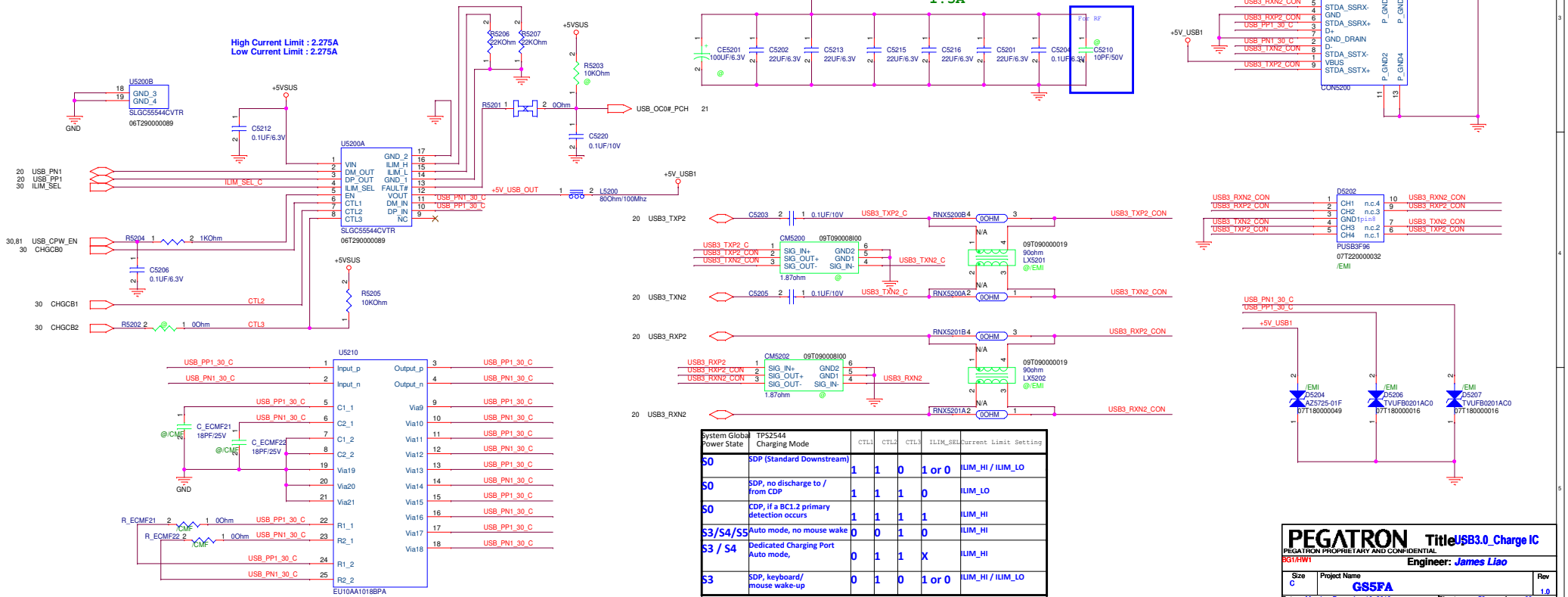
PEGATRON	Title: SATA/PCIE SSD		
SGT/HWT	Engineer: James Liao		
Size: Custom	Project Name: GS5FA		Rev: 1.0
Date: Monday, December 10, 2018	Sheet 51 of 98		

52 USB3.0



USB 3.0 ports x 1 with Sleep & Charge Left_Down

Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)



System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3 / S4	Dedicated Charging Port Auto mode,	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: USB3.0_Charge IC

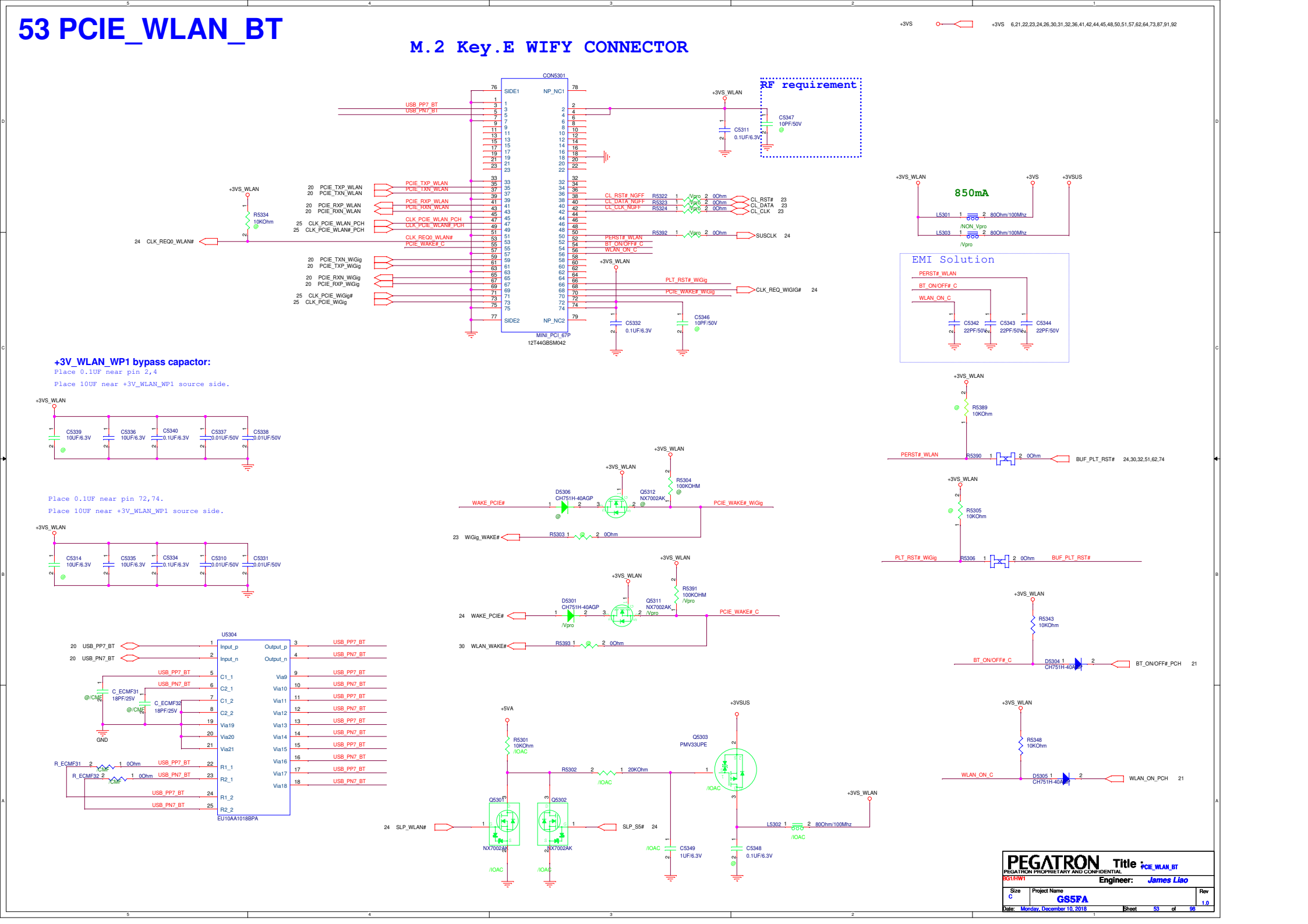
Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 52 of 98

53 PCIE_WLAN_BT

M.2 Key.E WIFY CONNECTOR



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.

Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.

PEGATRON Title : PCIE_WLAN_BT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: James Liao

Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 53 of 98

PEGATRON Title : G-Sensor

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1

Engineer: James Liao

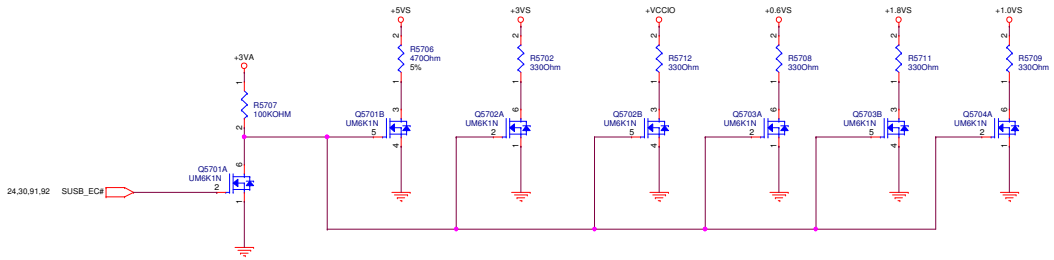
Size	Project Name	Rev
B	GS5FA	1.0

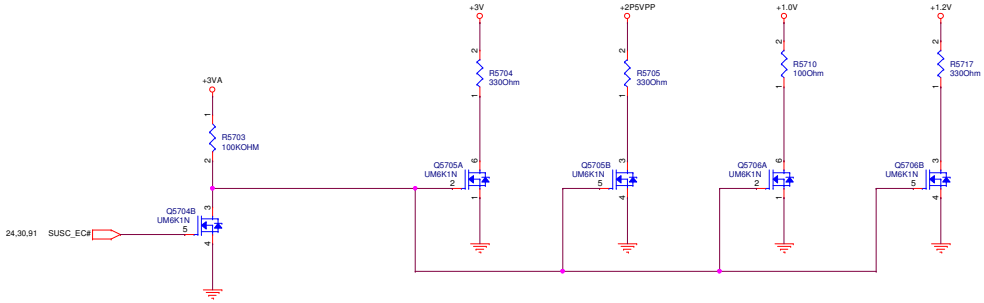
Date: Monday, December 10, 2018 Sheet 54 of 98

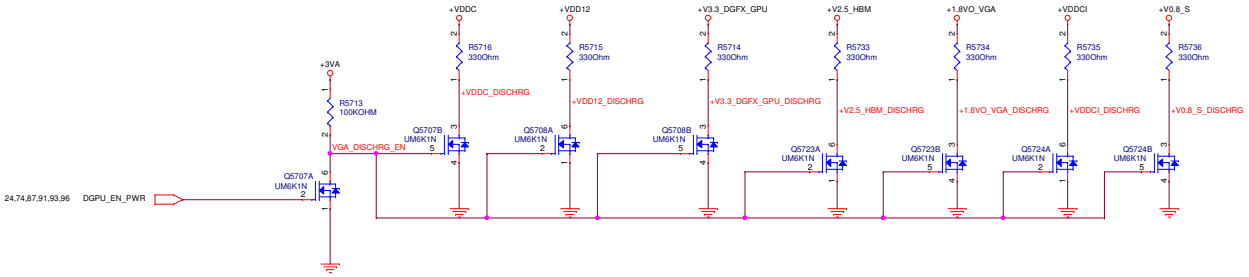
Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 55 of 98

PEGATRON
CONFIDENTIAL
Title: SATA SSD_HDD
Engineer: James Liao
Size: D
Project Name: G55FA
Rev: 1.0
Date: Monday, December 10, 2018
Sheet 56 of 99

57 DISCHARGE







+3VA
+5VS
+3VS
+VCCIO
+0.6VS
+1.8VS
+1.0VS

+3VA 26,30,31,36,67,81,88,93
+5VS 31,36,41,48,50,64,69,80,87,91
+3VS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,50,51,53,62,64,73,87,91,92
+VCCIO 3,5,9,94
+0.6VS 15,83
+1.8VS 22,36,74,91
+1.0VS 9,91

+3V
+1.0V
+2P5VPP
+1.2V

+3V 31,41,91
+1.0V 6,9,24,80,91
+2P5VPP 16,17,82
+1.2V 6,9,15,16,17,19,24,48,83

+VDDC
+VDD12
+V3.3_DGFX_GPU
+V2.5_HBM
+1.8VO_VGA
+VDDCI
+V0.8_S

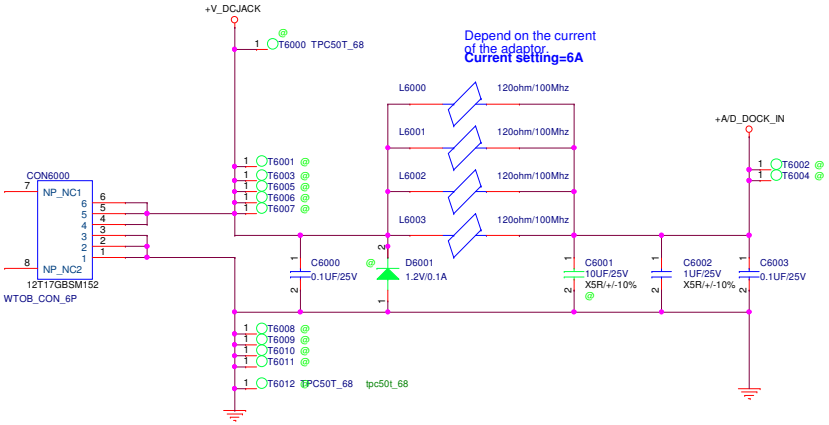
+VDDC 75,87
+VDD12 7,75,87
+V3.3_DGFX_GPU 24,72,73,74,75,91
+V2.5_HBM 74,75,95
+1.8VO_VGA 74,96
+VDDCI 75,89
+V0.8_S 75,86

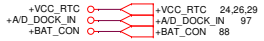
PEGATRON Title : DISCHARGE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGT/HWT Engineer: James Liao
Size Custom | Project Name GS5FA | Rev 1.0
Date: Monday, December 10, 2018 | Sheet 57 of 98

Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 58 of 98

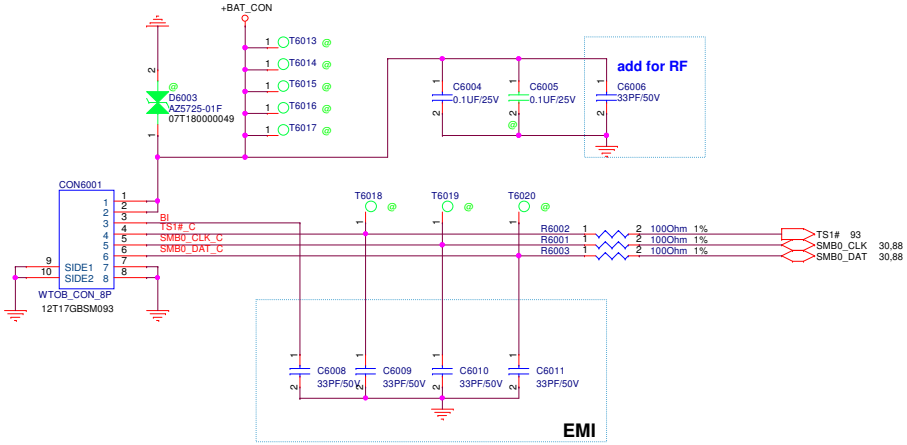
Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 59 of 98

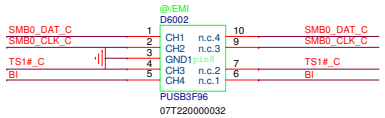
60 DC_BAT_CONN

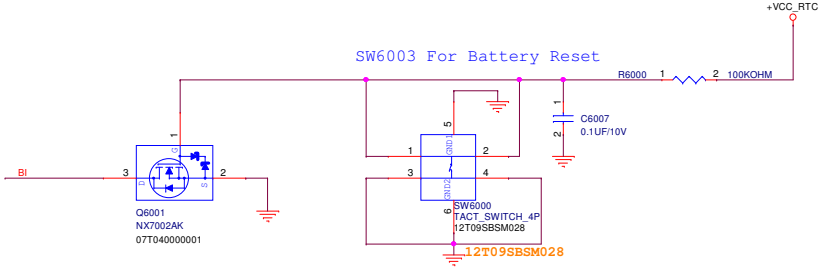




Battery Connector







PEGATRON	Title : DC_BAT_CONN		
BG1/HW1	Engineer: James Liao		
Size: Custom	Project Name: GS5FA		Rev: 1.0
Date: Monday, December 10, 2018	Sheet 60 of 98		

PEGATRON Title : <Title>

BG1/HW1 Engineer: James Liao

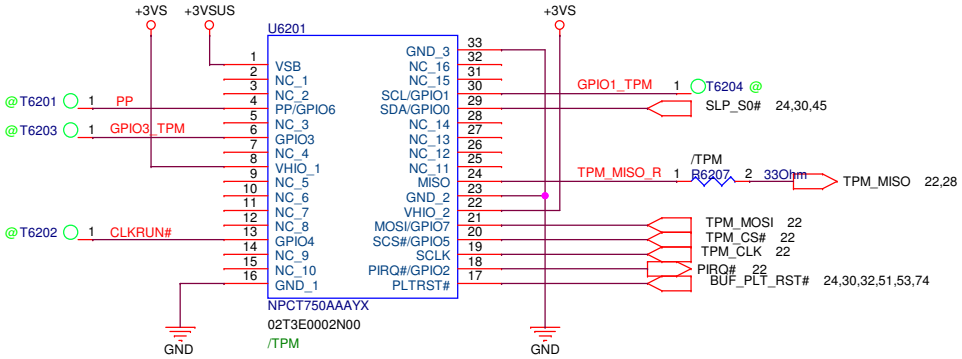
Size	Project Name	Rev
C	GS5FA	1.0

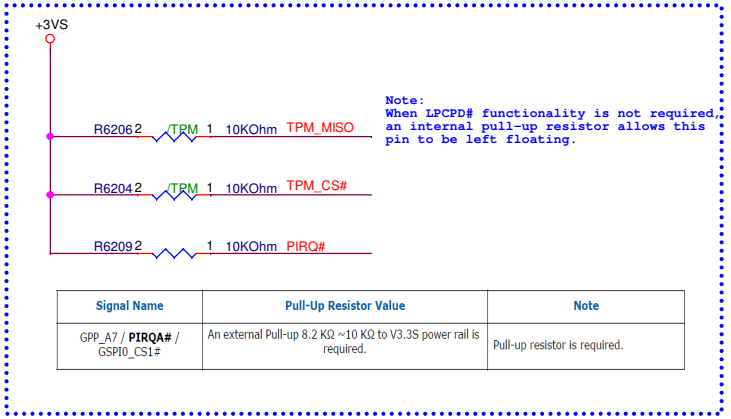
Date: Monday, December 10, 2018 Sheet 61 of 98

62 TPM NPCT750 - SPI

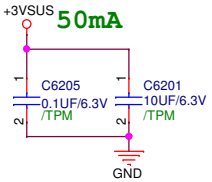
+3VS
+3VSUS

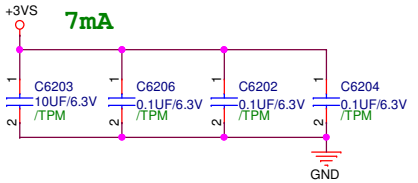
+3VS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,50,51,53,57,64,73,87,91,92
+3VSUS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,50,51,53,57,64,73,87,91,92





Signal Name	Pull-Up Resistor Value	Note
GPP_A7 / **PIRQA#** / GSPI0_CS1#	An external Pull-up 8.2 KΩ ~10 KΩ to V3.3S power rail is required.	Pull-up resistor is required.





PEGATRON Title : TPM NPCT650

BG1/HW1 Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 62 of 98

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PEGATRON

Title : USB 2.0 Hub

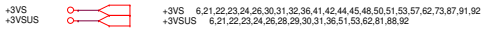
PEGATRON PROPRIETARY AND CONFIDENTIAL

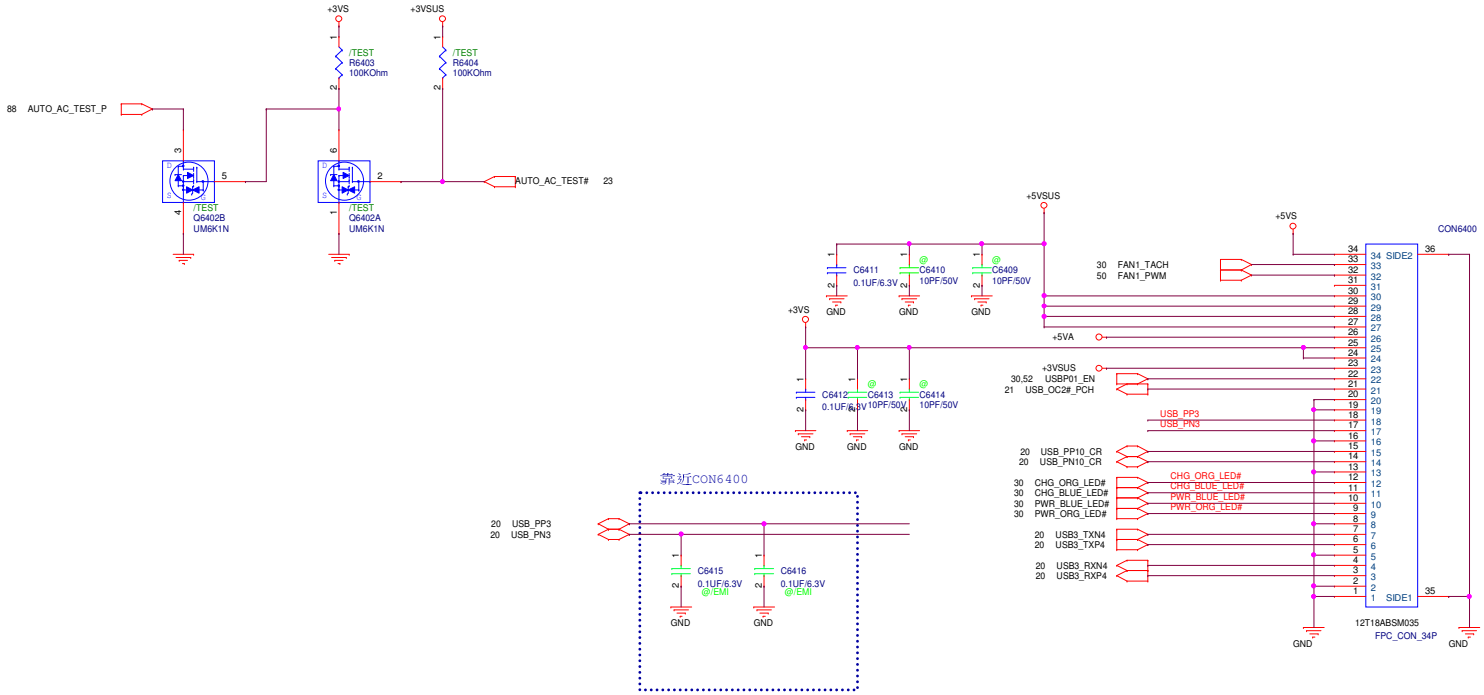
Engineer: James Liao

Size	Project Name	Rev
A	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 63 of 98

64 IO CONN





PEGATRON	Title : IO Board		
BG1/HW1	Engineer: James Liao		
Size: C	Project Name: GS5FA		Rev: 1.0
Date: Monday, December 10, 2018	Sheet 64 of 98		

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : IO BOARD LED SD

Engineer: *James Liao*

Size	Project Name	Rev
C	GS5FA	1.1

Date: Monday, December 10, 2018 Sheet 65 of 98

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : IO BOARD USB3.0

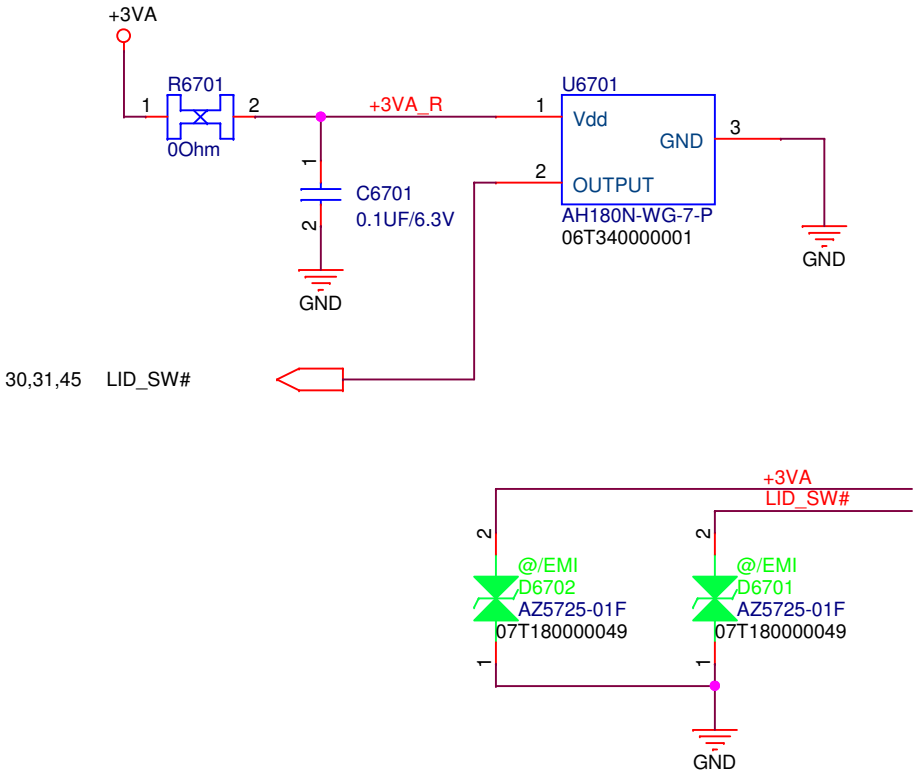
BG1/HW1

Engineer: *James Liao*

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 66 of 98

67 LID SW



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LID

BG1/HW1

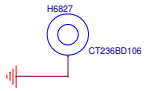
Engineer: *James Liao*

Size	Project Name	Rev
A	GS5FA	1.0

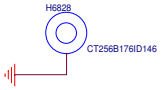
Date: Monday, December 10, 2018 Sheet 67 of 98

68 ME Hole

GPU bracket nut



SMT NUT FOR WIFI



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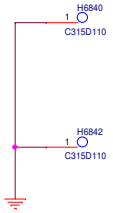

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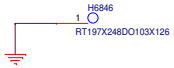

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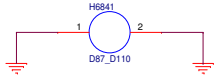

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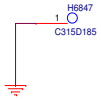
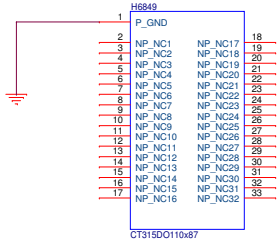
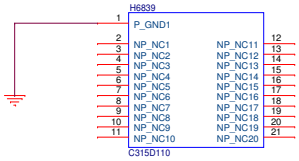
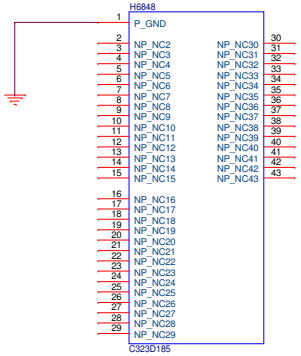
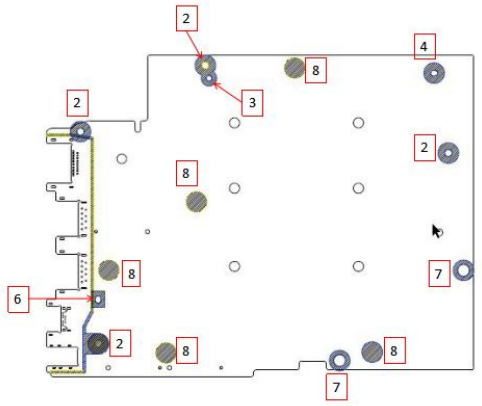
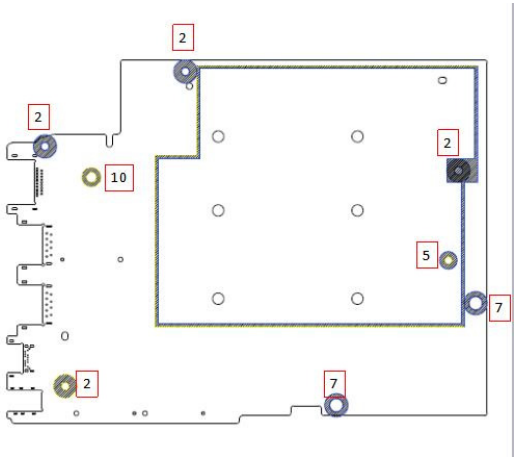




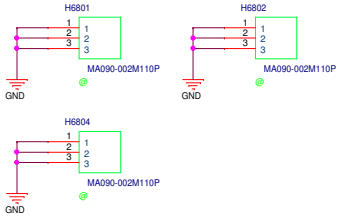




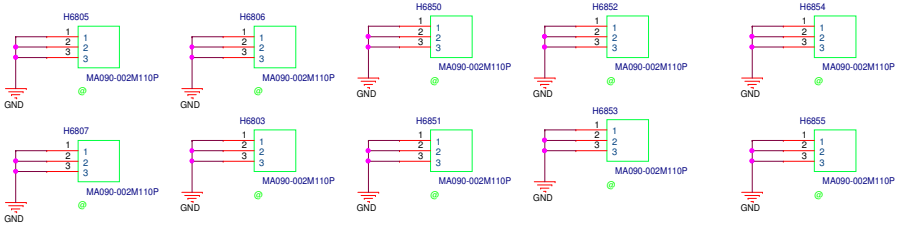




IO Clip(TOP)



CPU Clip(BOT)



PEGATRON Title : ME Hole

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: James Liao

BG1/HW1

Size	Project Name	Rev
C	GS5FA	1.0

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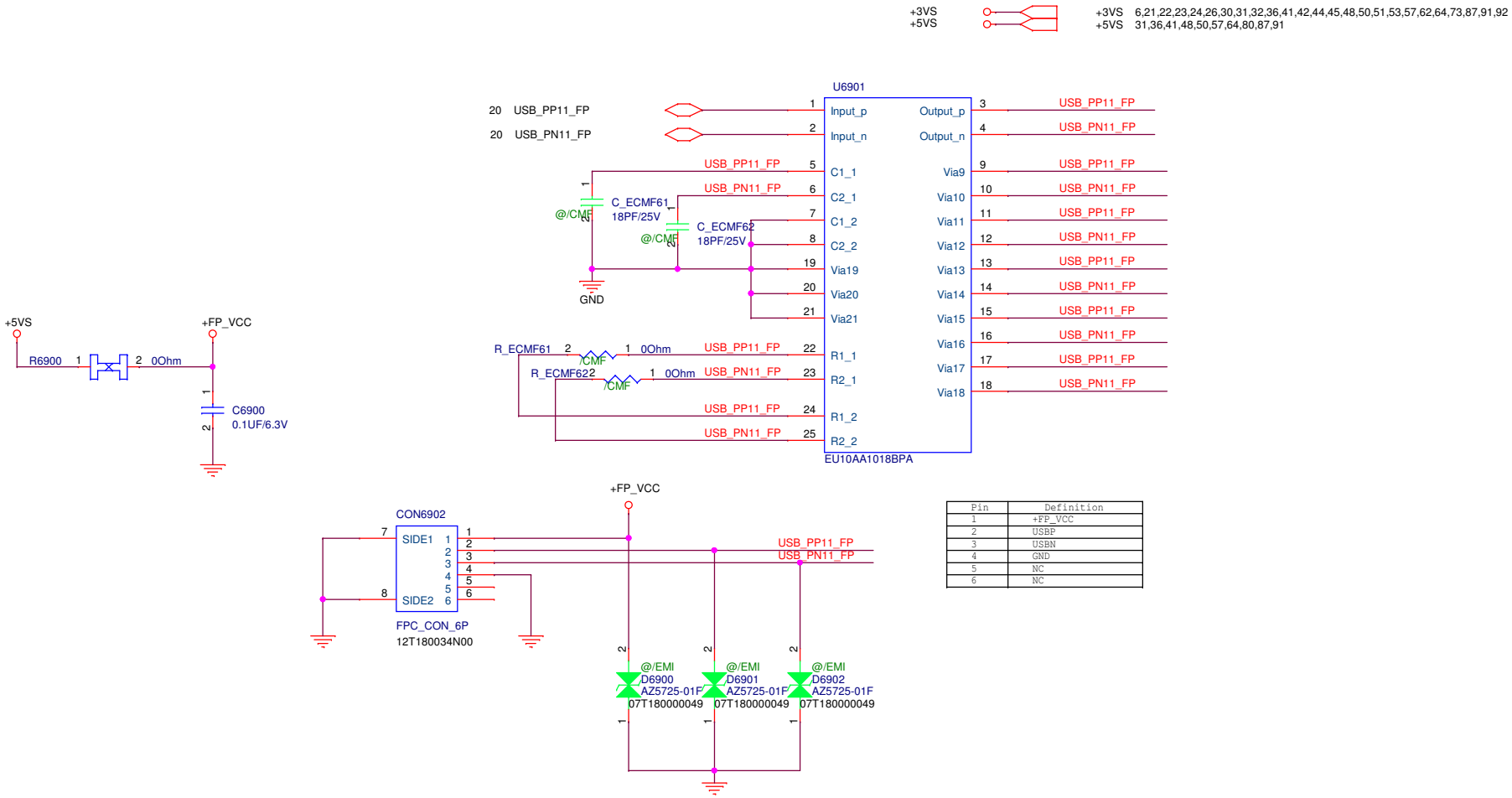
69 FP



Pin	Definition
1	+FP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW1

Title : Finger printer
Engineer: James Liao

Size	Project Name	Rev
B	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 69 of 98

PEGATRON

Title : GPU-PCIE

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW1

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 70 of 98

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU_FRAME BUFF

BG1-HW1

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

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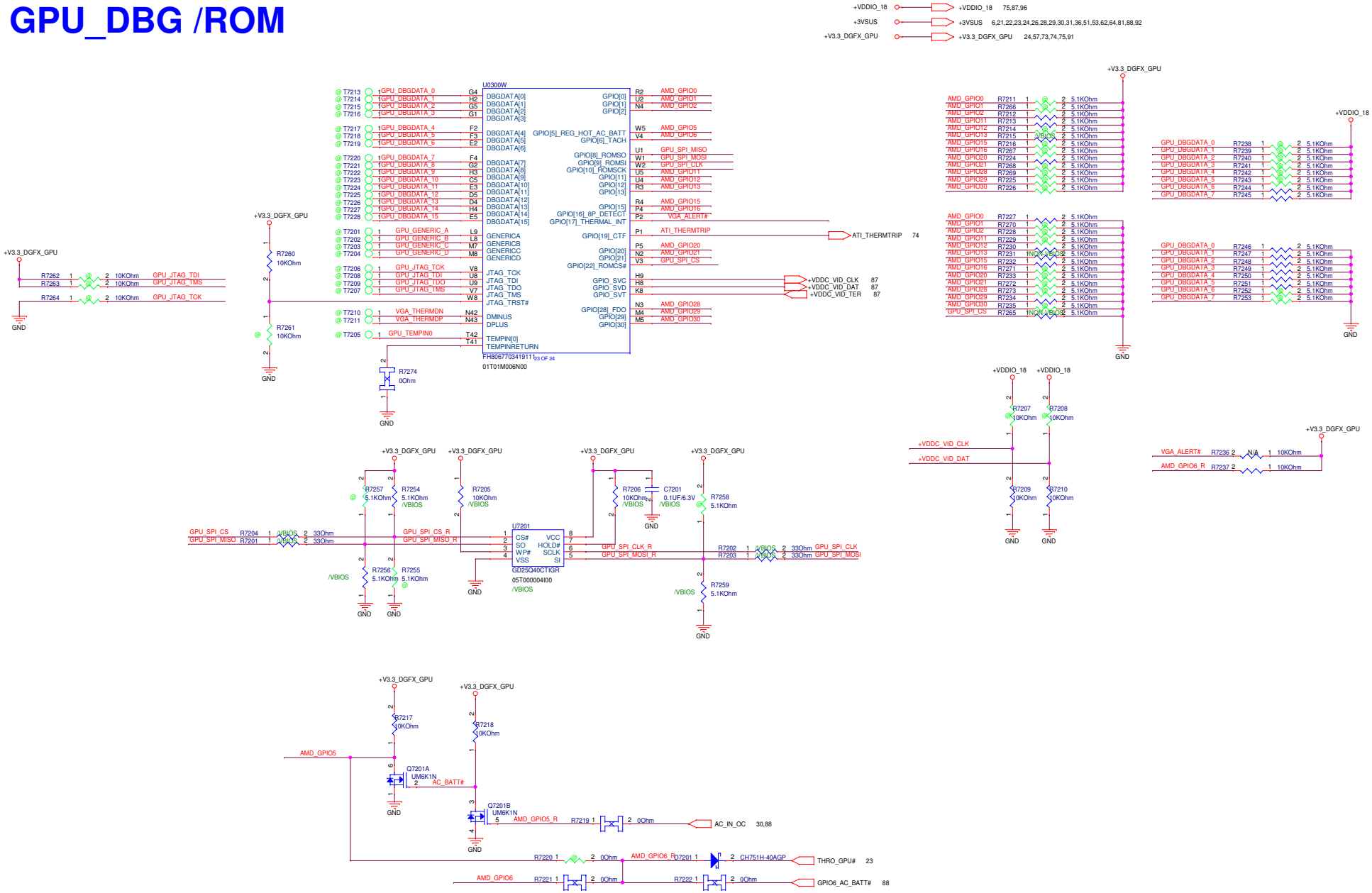
72 GPU_DBG /ROM



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW1
Engineer: James Liao

Title : GPU_DBG /ROM

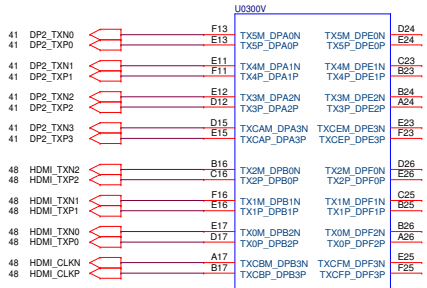
Size	Project Name	Rev
C	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 72 of 98

73 GPU_DP/HDMI

Type C DP

HDMI

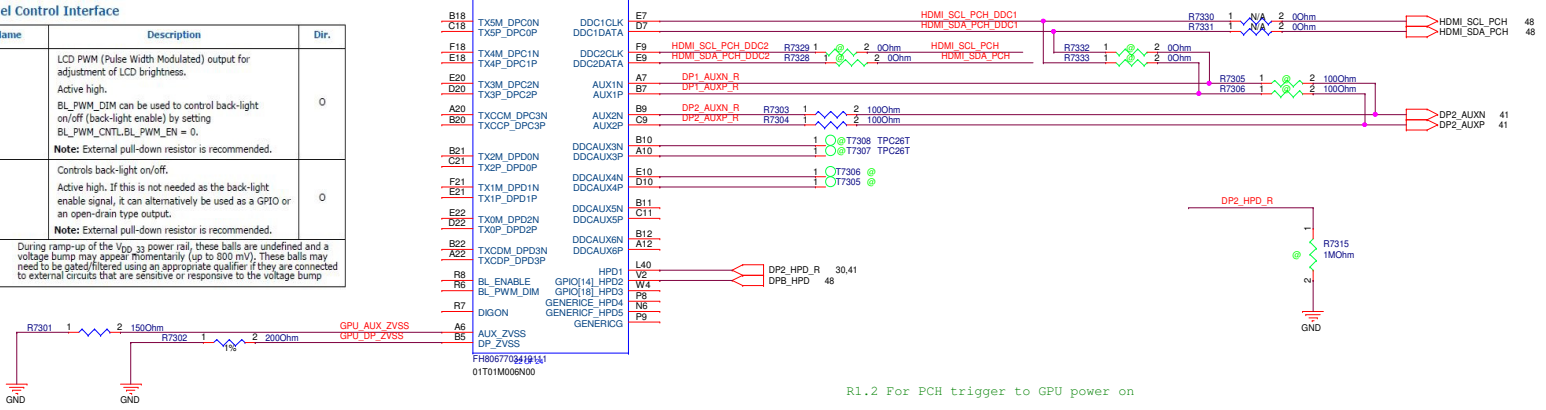


R1.1 Change DP AUX Port

R1.4 預留DDC2/AUX1 for HDMI/DP

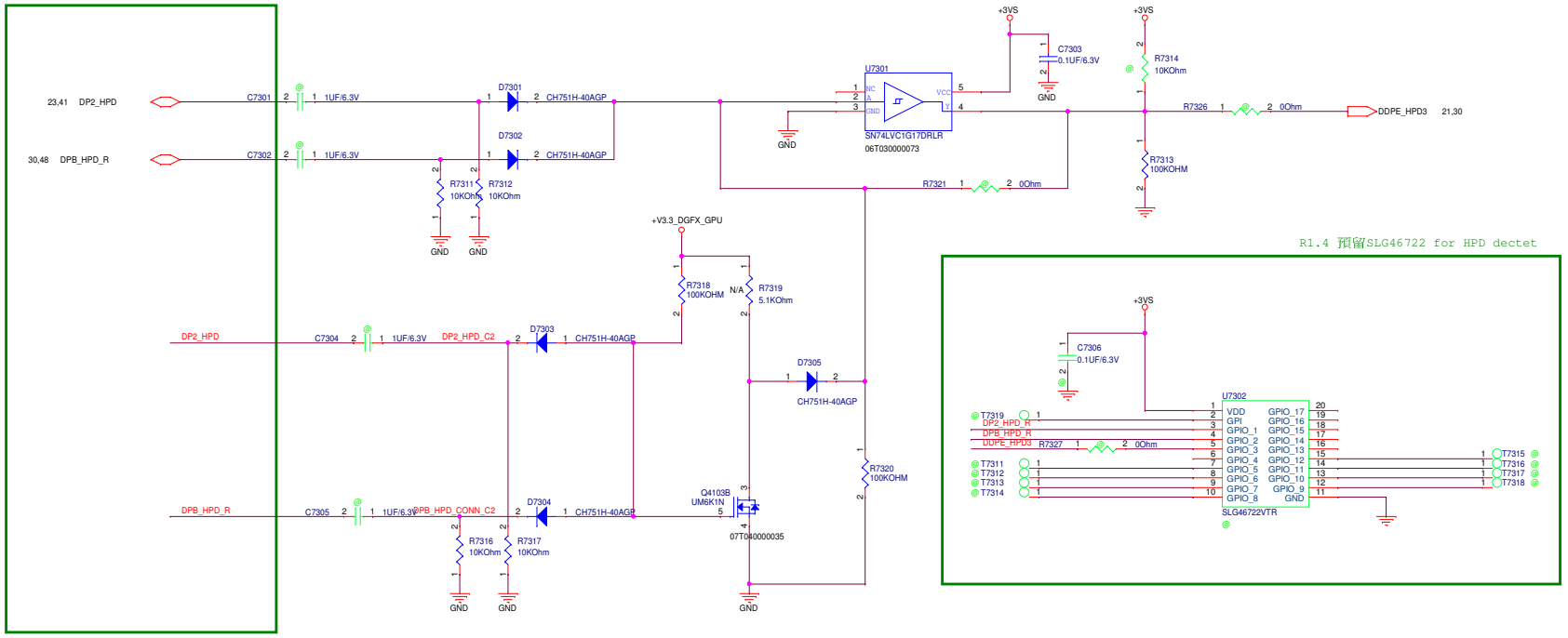
Table 6-26. dGPU Panel Control Interface

Signal Name	Description	Dir.
BL_PWM_DIM	LCD PWM (Pulse Width Modulated) output for adjustment of LCD brightness. Active high. BL_PWM_DIM can be used to control back-light on/off (back-light enable) by setting BL_PWM_CNTL.BL_PWM_EN = 0. **Note:** External pull-down resistor is recommended.	O
BL_ENABLE	Controls back-light on/off. Active high. If this is not needed as the back-light enable signal, it can alternatively be used as a GPIO or an open-drain type output. **Note:** External pull-down resistor is recommended.	O
Note:	During ramp-up of the V_{DD_33} power rail, these balls are undefined and a voltage bump may appear momentarily (up to 800 mV). These balls may need to be gated/filtered using an appropriate qualifier if they are connected to external circuits that are sensitive or responsive to the voltage bump	



R1.2 For PCH trigger to GPU power on

R1.4 修改Dispaly HPD input



R1.4 預留SLG46722 for HPD dectet

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU_DP_HDMI

BG1-HW1

Engineer: *James Liao*

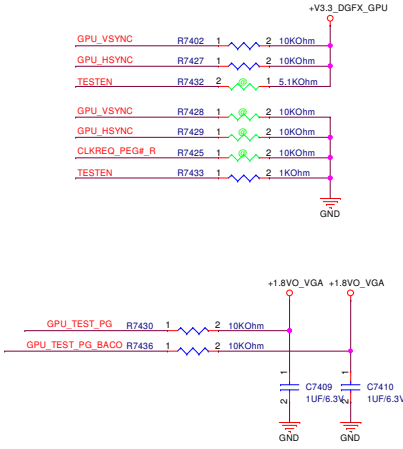
Size	Project Name	Rev
C	GS5FA	1.0

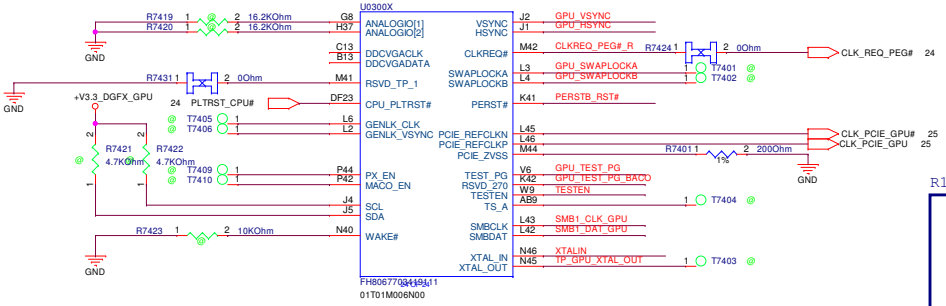
Date: Thursday, December 13, 2018 Sheet 73 of 98

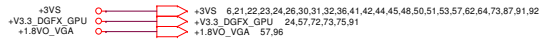
74 GPU_SEQ/ XTAL

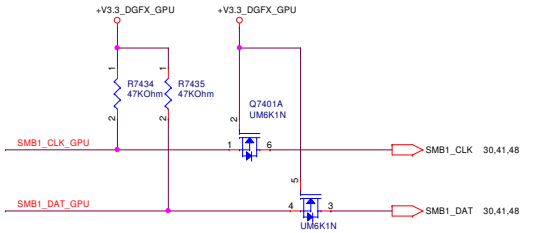
Table 6-28. dGPU Miscellaneous Signals Interface

Signal Name	Description	Dir.	Link Type	Notes
PX_EN	On/off regulator switch in switchable graphics BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is de-asserted. Can be left unconnected if not used.	O	SE	1
MACO_EN	Can be used as logic control for GPU memory self refresh	O	TBD	-
Note:				
1) Switchable Graphics BACO mode is not supported in KBL G application.				

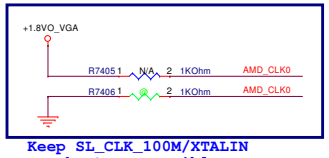


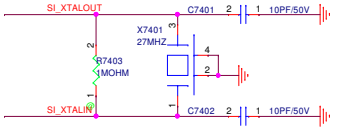






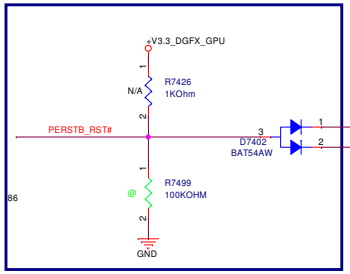
R1.1 mount R7406/unmount R7405



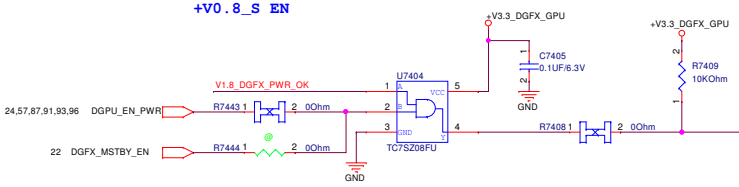


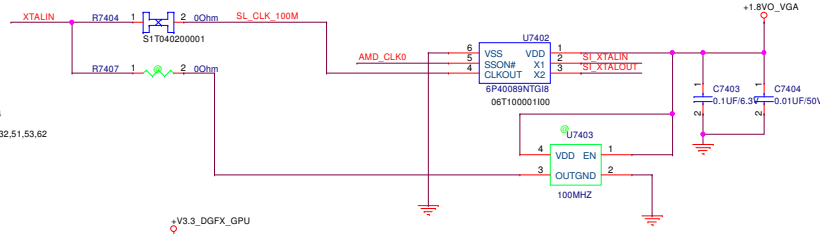
Keep SL_CLK_100M/XTALIN as short as possible

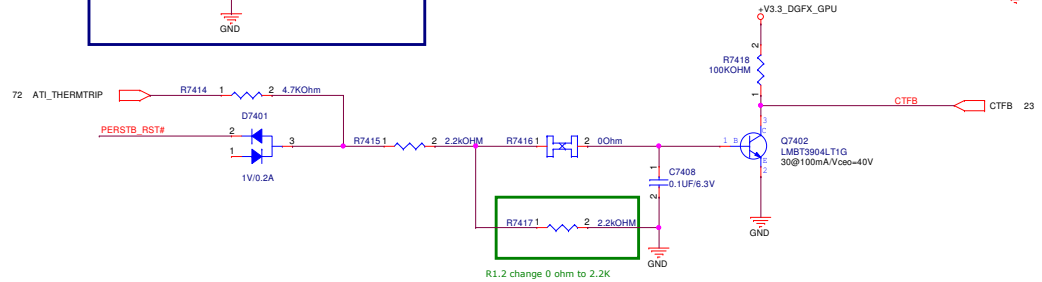
R1.1 mount R7426/unmount R7499



+V0.8_S EN

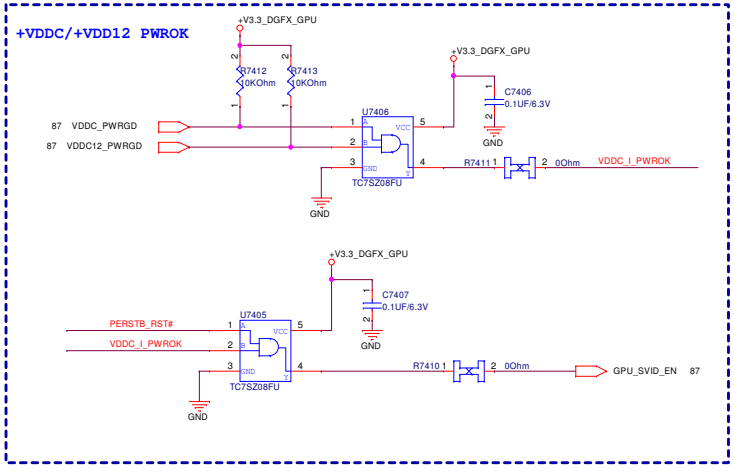




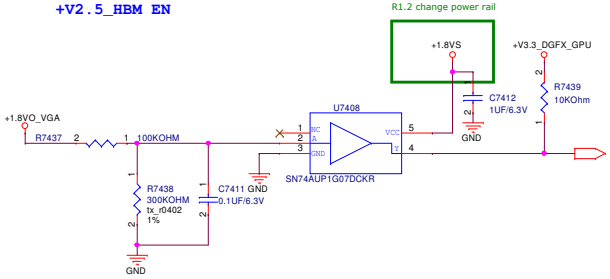


R1.2 change 0 ohm to 2.2K

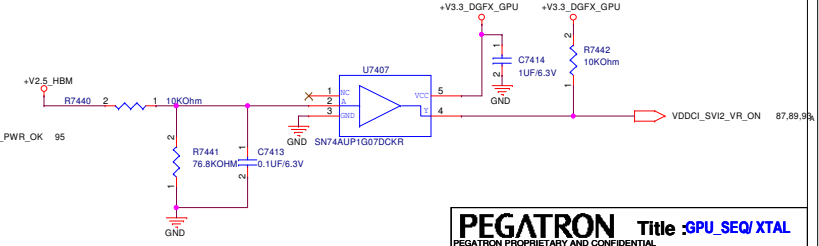
+VDDC/+VDD12 PWROK



+V2.5_HBM EN



+VDDC/+VDD12 EN



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :GPU_SEQ/ XTAL

BG1-HW1

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

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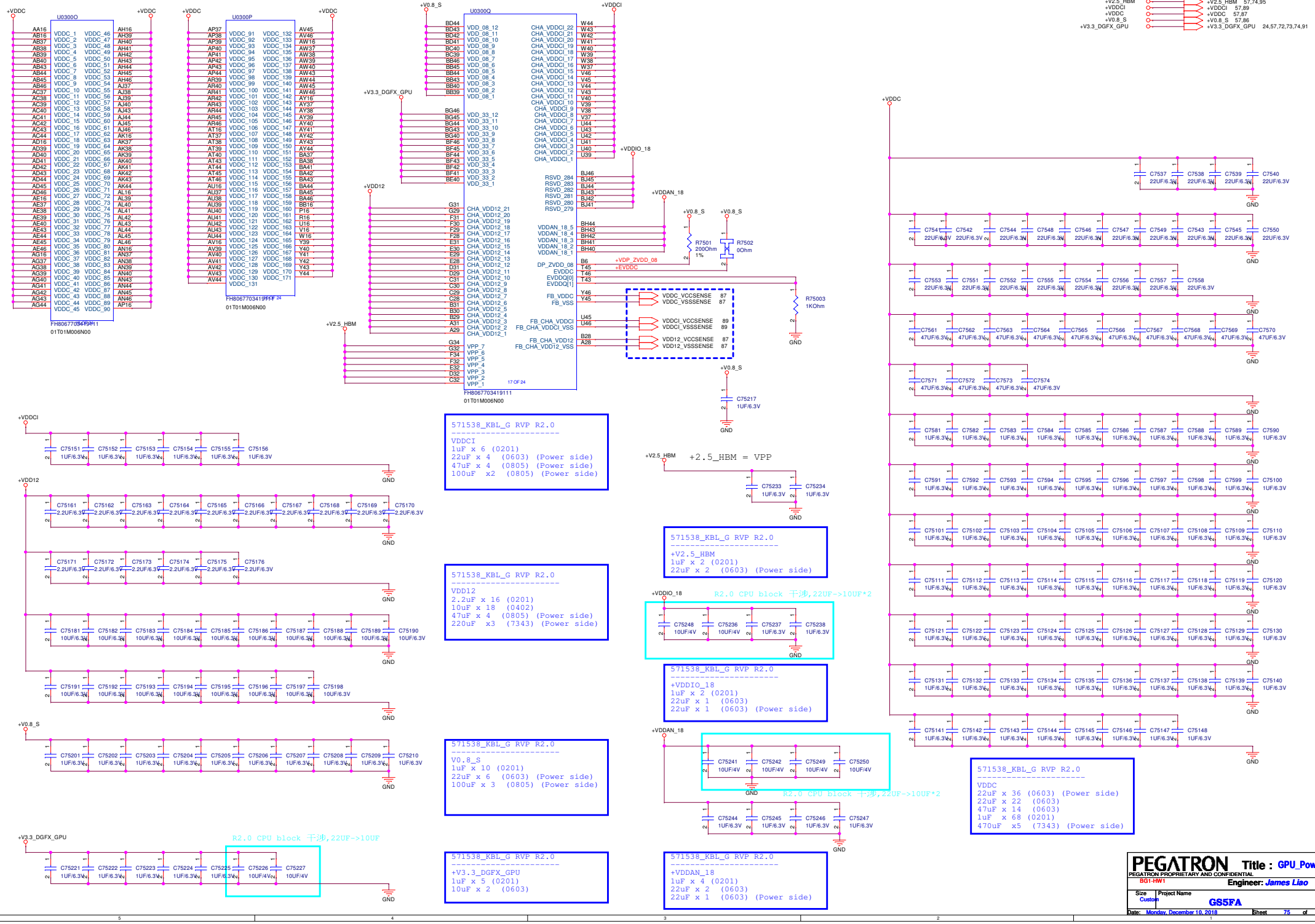
75 GPU_POWER



+VDDIO_18	+VDDIO_18	72,87,96
+VDDAN_18	+VDDAN_18	7,96
+VDD12	+VDD12	7,57,87
+V2.5_HBM	+V2.5_HBM	57,74,95
+VDDCI	+VDDCI	57,89
+VDDC	+VDDC	57,87
+V0.8_S	+V0.8_S	57,86
+V3.3_DGFX_GPU	+V3.3_DGFX_GPU	24,57,72,73,74,91

Title :	GPU_Power,GND	
Engineer:	James Liao	
Size	Project Name	Rev
Custom	G5SFA	1.0
Date:	Monday, December 10, 2018	Sheet 75 of 98

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW1

PEGATRON

Title : GDDR5 X32 *A

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW1

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Monday, December 10, 2018 Sheet 76 of 98

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GDDR5 X32 *B

BG1-HW1

Engineer: James Liao

Size	Project Name	Rev
Custom	GS5FA	1.0

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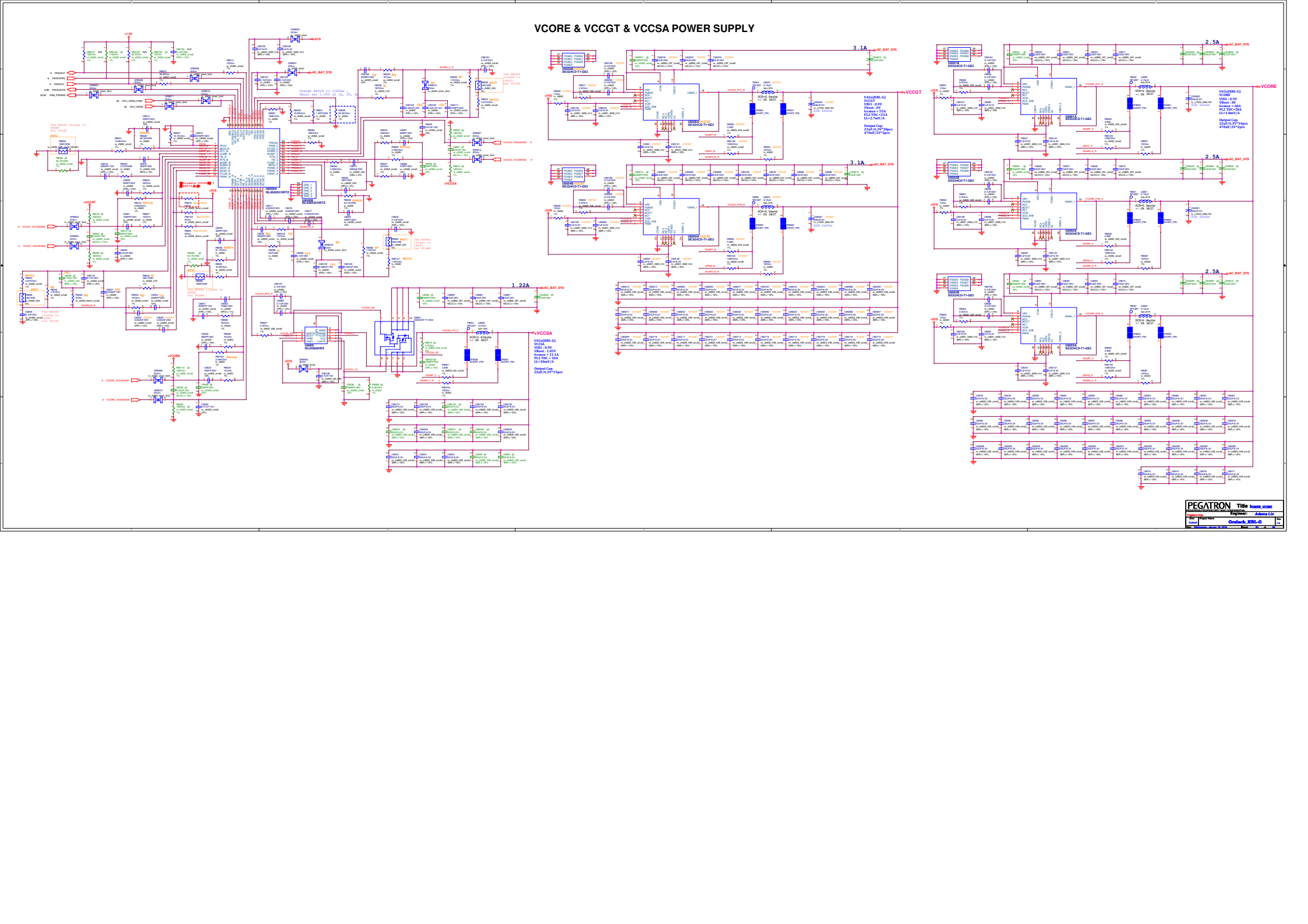
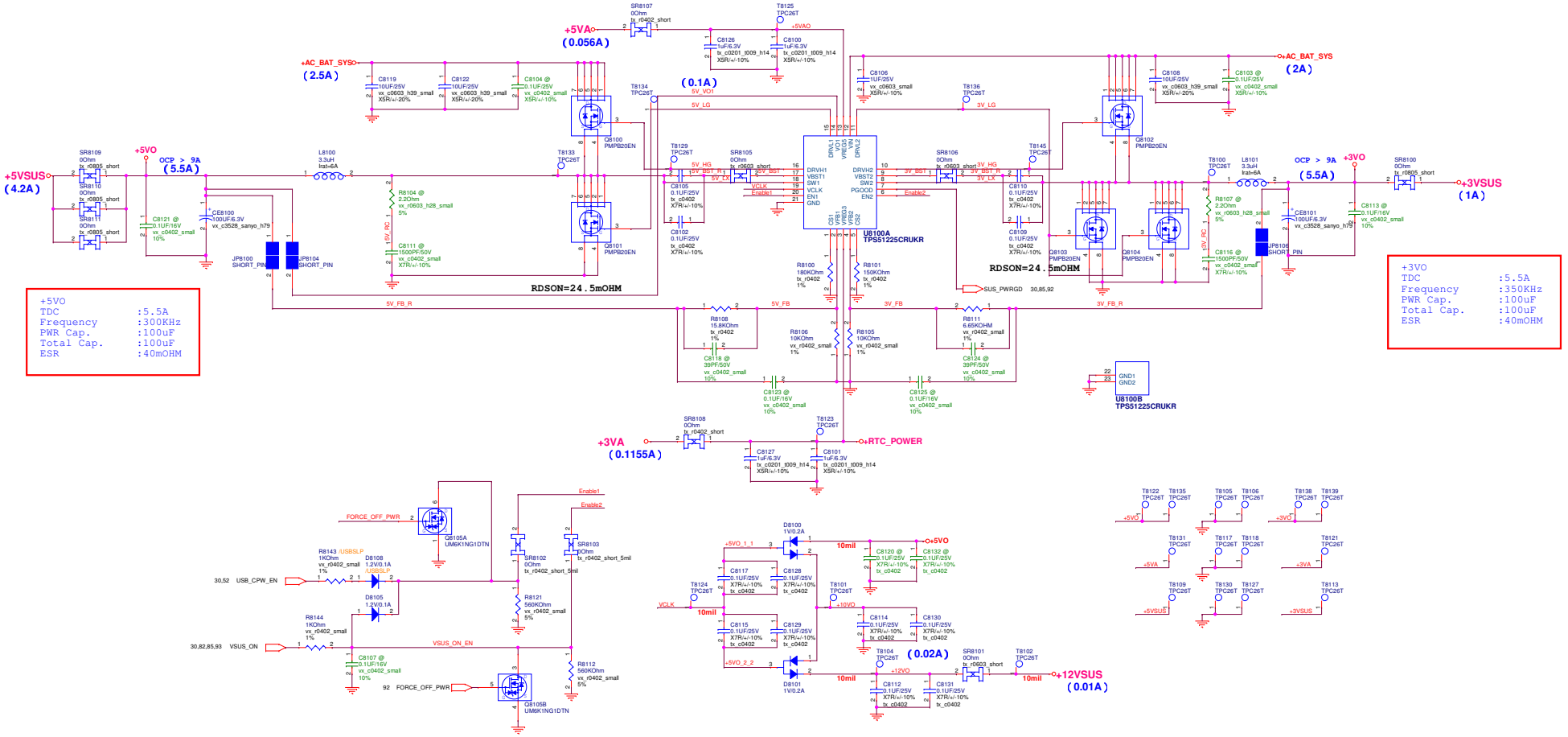
Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 78 of 98

Title	<Title>
Size: A	Document Number: GS5FA
Rev: 1.0	
Date: Monday, December 10, 2018	Sheet 79 of 98

VCORE & VCCGT & VCCSA POWER SUPPLY

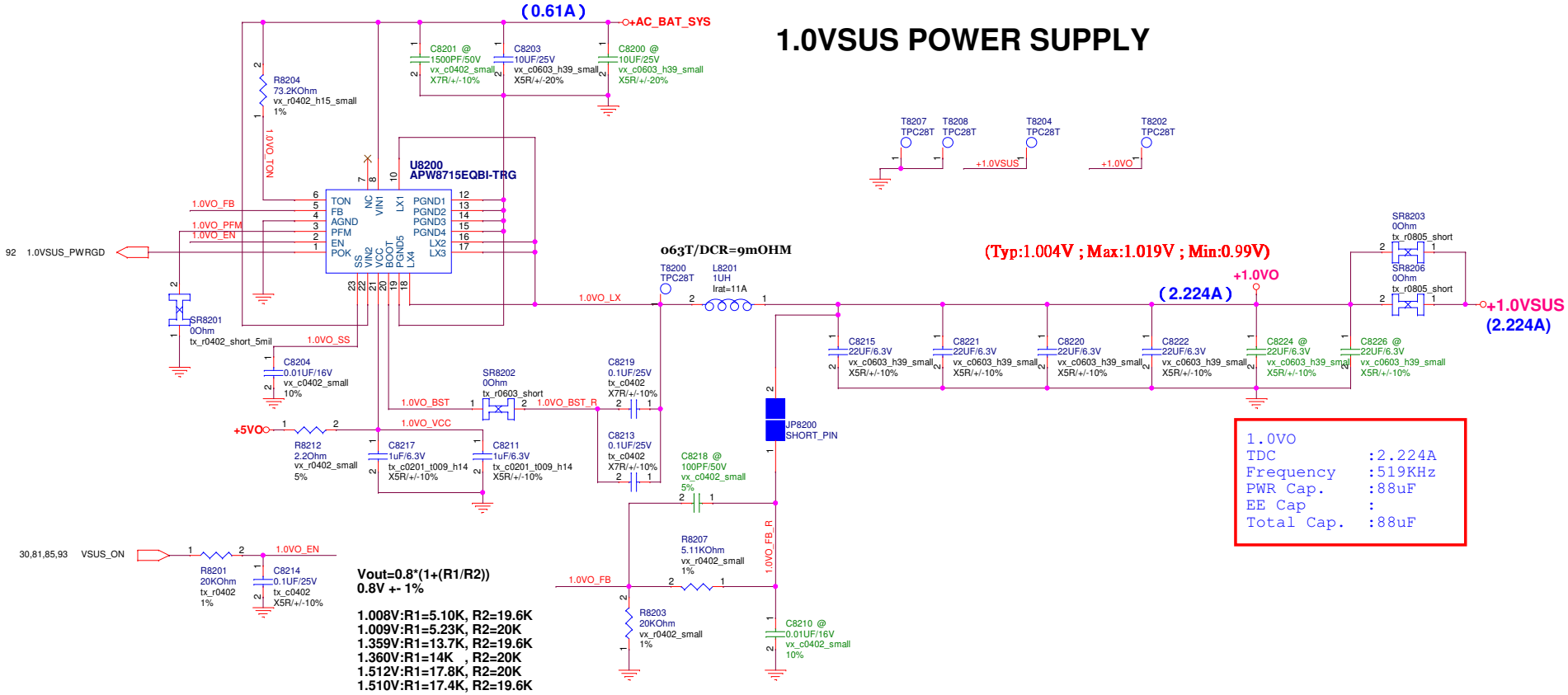


5VO & 3VO POWER SUPPLY



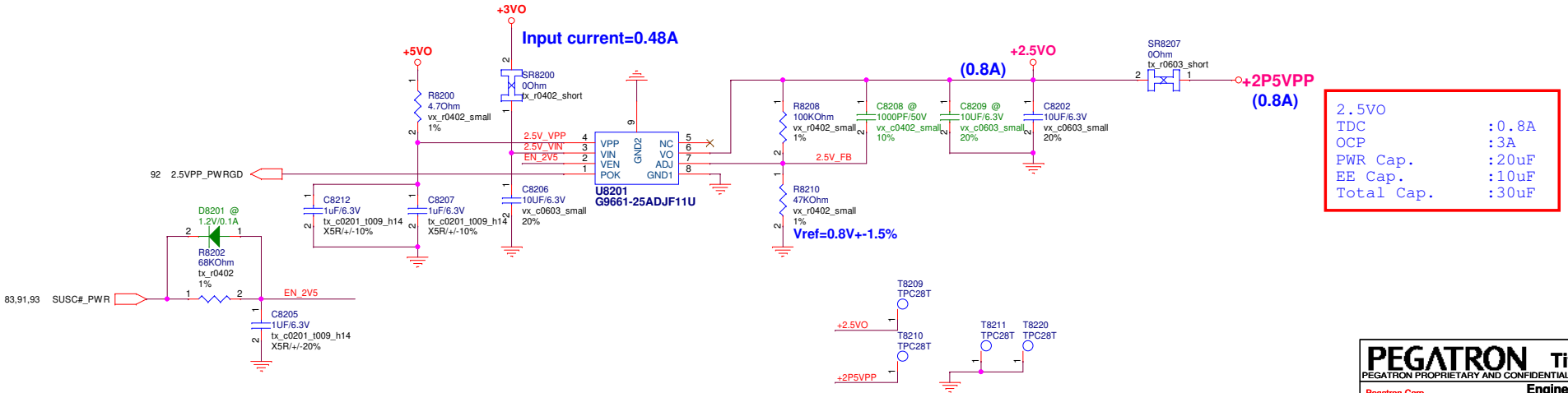
PEGATRON	Title: POWER_SYSTEM
PEGATRON PROPRIETARY AND CONFIDENTIAL	
Pegatron Corp.	Engineer: Adams Lin
Size: Custom	Project Name: Grolsch_KBL-G
Rev: 1.0	
Date: Friday, December 28, 2018	Sheet 81 of 98

1.0VSUS POWER SUPPLY



1.0VO	
TDC	:2.224A
Frequency	:519KHz
PWR Cap.	:88uF
EE Cap	:
Total Cap.	:88uF

2.5V POWER SUPPLY



2.5VO	
TDC	:0.8A
OCP	:3A
PWR Cap.	:20uF
EE Cap.	:10uF
Total Cap.	:30uF

PEGATRON Title :P82_+1.0VSUS & +2.5V

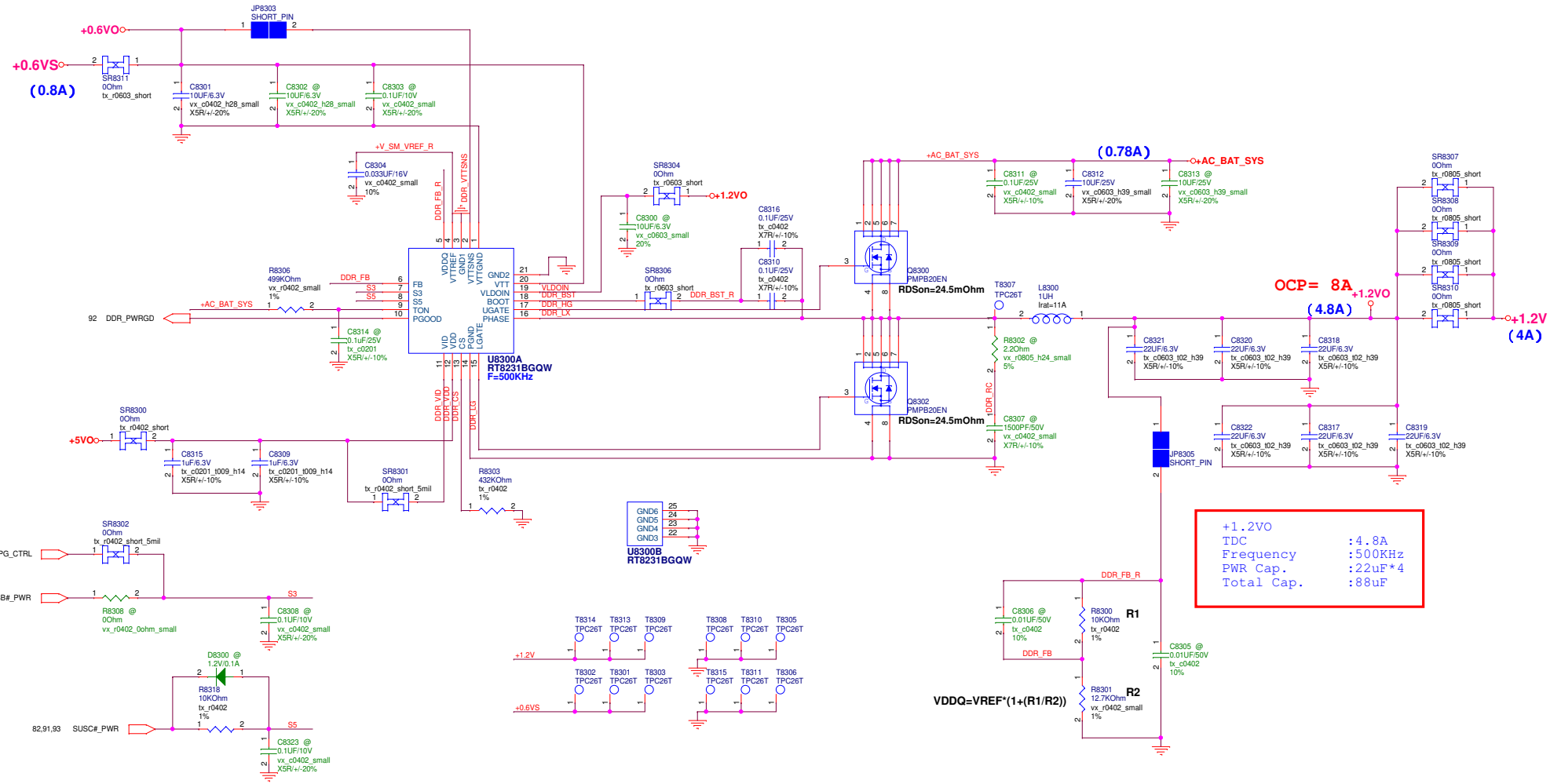
PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: Adams Lin

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Friday, December 28, 2018 Sheet 82 of 98

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON Title :POWER_DDR & VTT
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Adams Lin
Size: Custom | Project Name: Grolsch_KBL-G | Rev: 1.0
Date: Friday, December 28, 2018 Sheet 83 of 98

PEGATRON

Title :Power N/A

PEGATRON PROPRIETARY AND CONFIDENTIAL

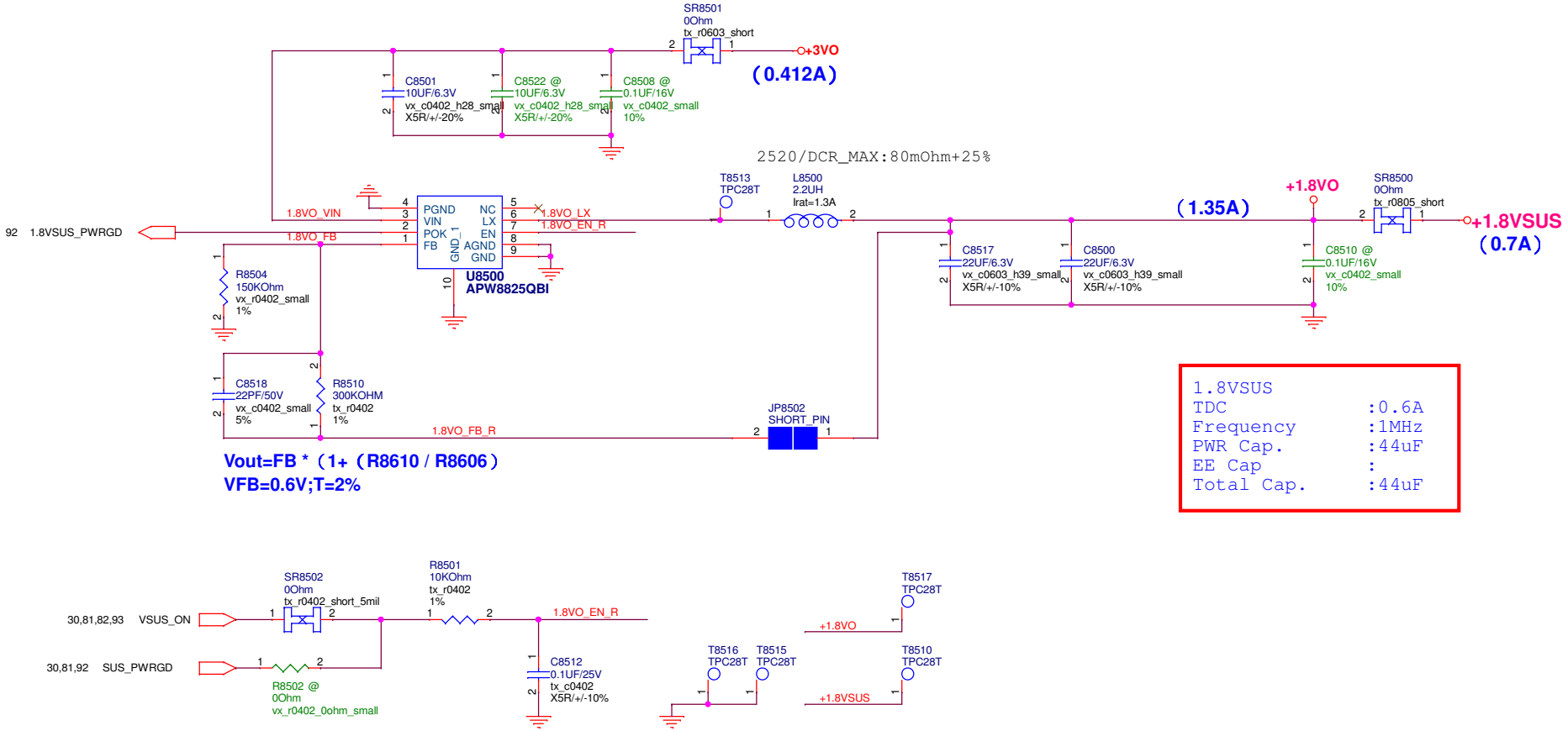
Pegatron Corp.

Engineer: Adams Lin

Size	Project Name	Rev
B	Grolsch_KBL-G	1.0

Date: Friday, December 28, 2018 Sheet 84 of 98

1.8VSUS POWER SUPPLY



PEGATRON Title : p. 85_+1.8VSUS

PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: Adams Lin

Size	Project Name	Rev
Custom	Grolsch_KBL-G	1.0

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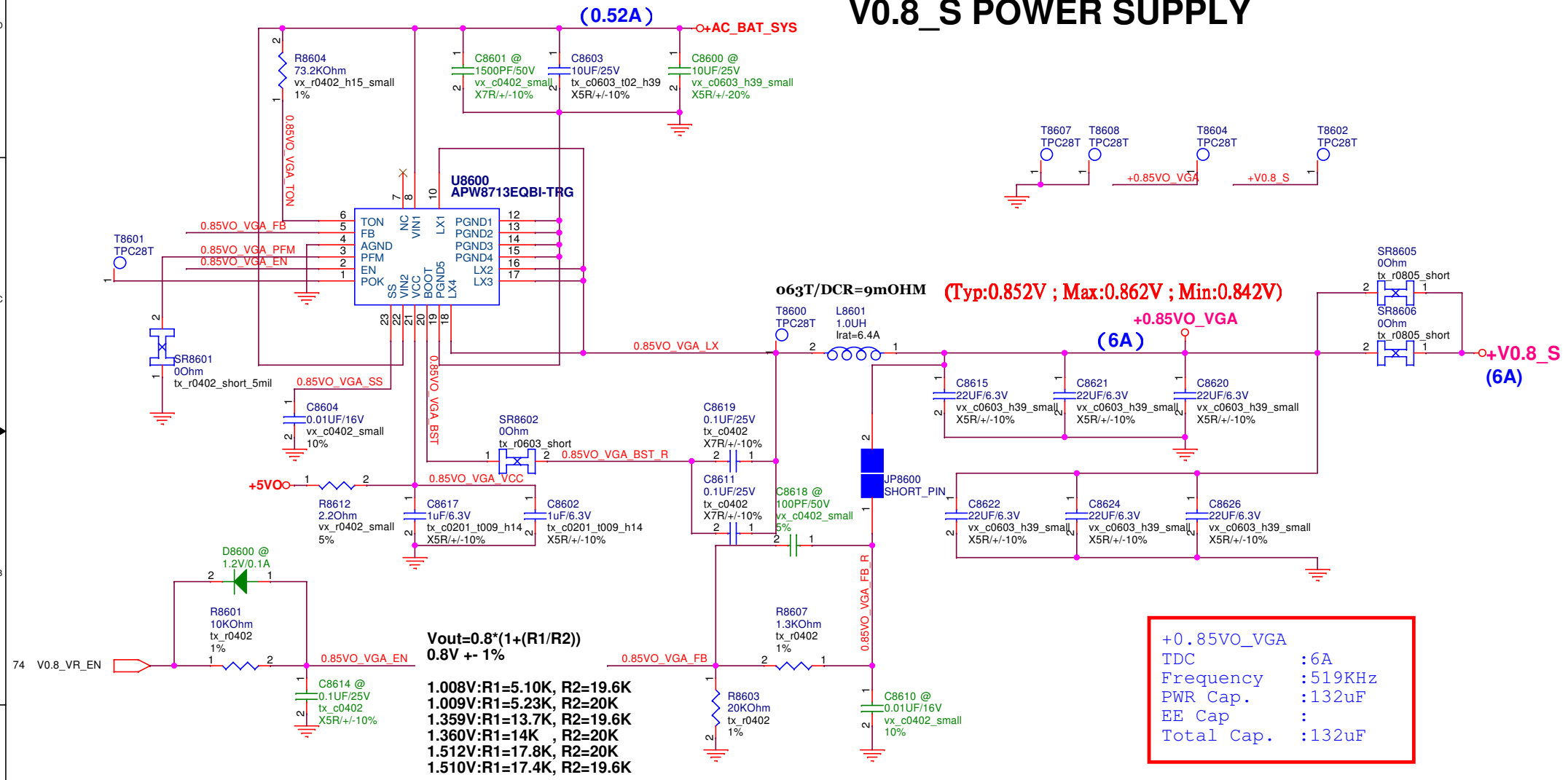
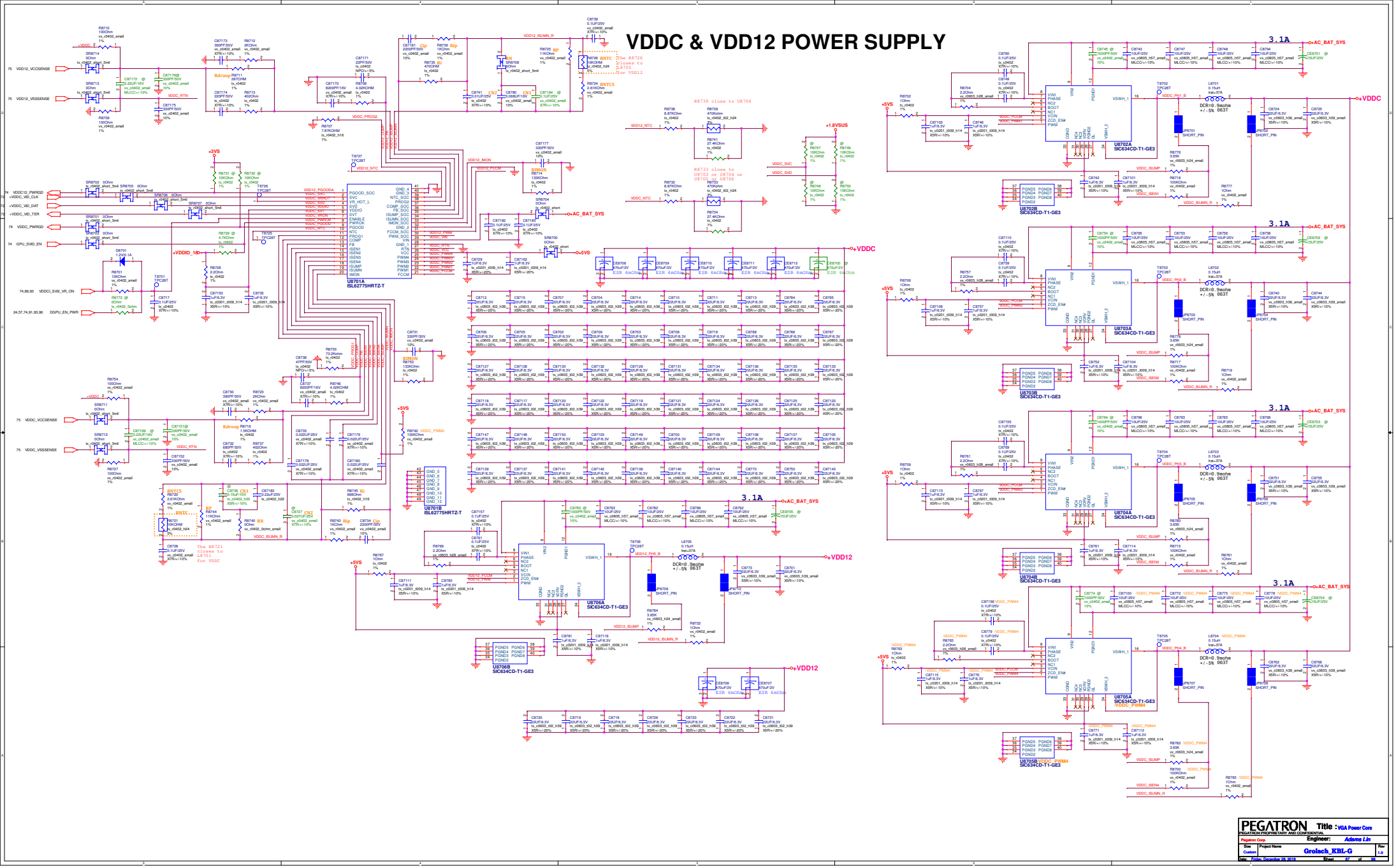
V0.8_S POWER SUPPLY



+0.85VO_VGA
TDC :6A
Frequency :519KHz
PWR Cap. :132uF
EE Cap :
Total Cap. :132uF

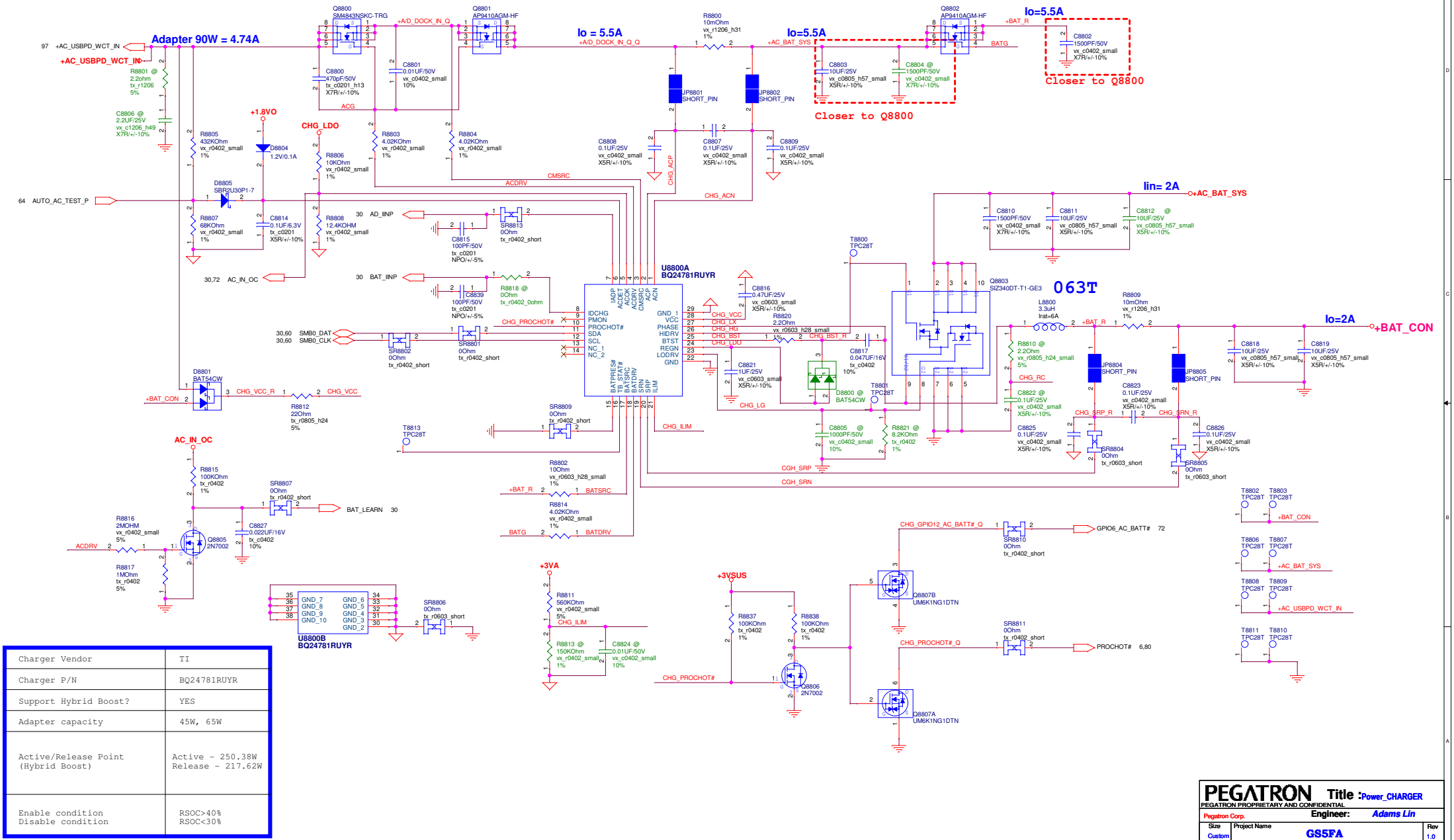
PEGATRON Title :Power_V0.8_S
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Adams Lin
Size: Custom | Project Name: GS5FA | Rev: 1.0
Date: Friday, December 28, 2018 Sheet 86 of 98

VDDC & VDD12 POWER SUPPLY



PEGATRON Title : VGA Power Core
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Adams Lin
Size: Custom | Project Name: Groisch_KBL-G | Rev: 1.0
Date: Friday, December 28, 2018 Sheet 87 of 98

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24781RUYR
Support Hybrid Boost?	YES
Adapter capacity	45W, 65W
Active/Release Point (Hybrid Boost)	Active - 250.38W Release - 217.62W
Enable condition Disable condition	RSOC>40% RSOC<30%

PEGATRON Title : Power_CHARGER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: Adams Lin

Size	Project Name	Rev
Custom	GS5FA	1.0

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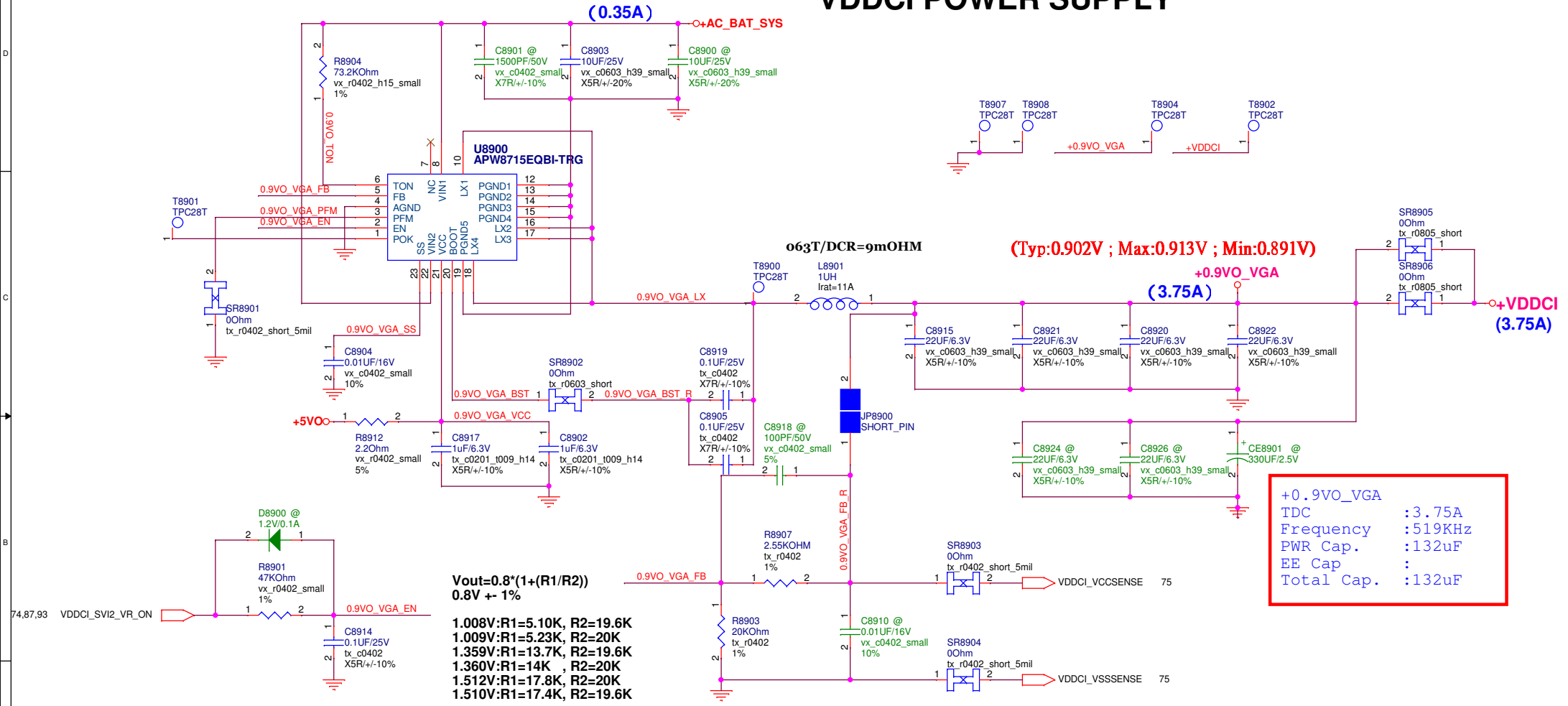
VDDCI POWER SUPPLY



PEGATRON	Title : Power_VDDCI		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Pegatron Corp.	Engineer: Adams Lin		
Size: Custom	Project Name: GS5FA		Rev: 1.0
Date: Friday, December 28, 2018	Sheet 89 of 98		

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power N/A

Pegatron Corp.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	Grolsch_KBL-G	1.0

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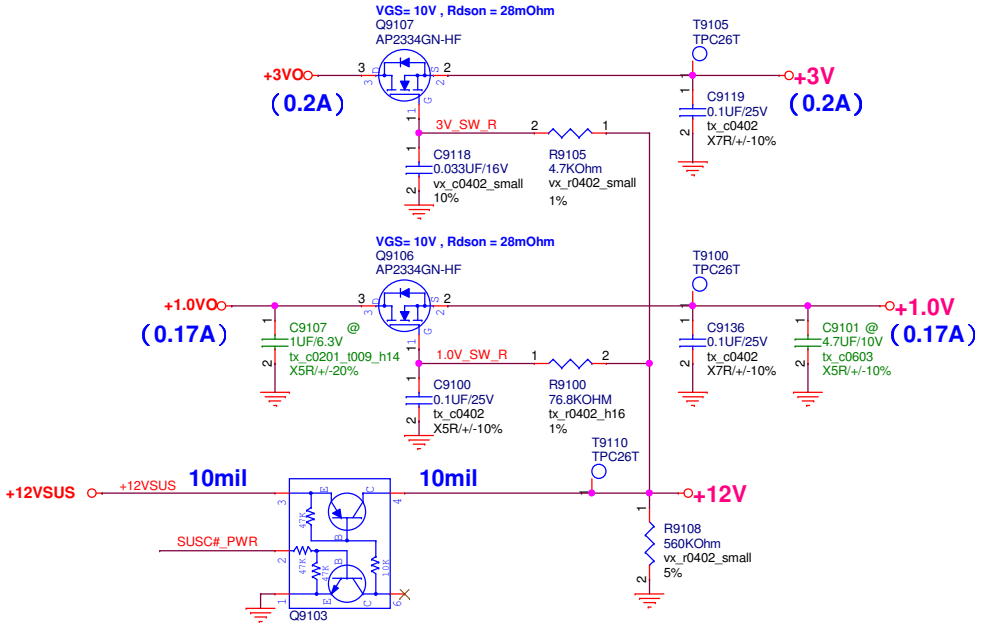
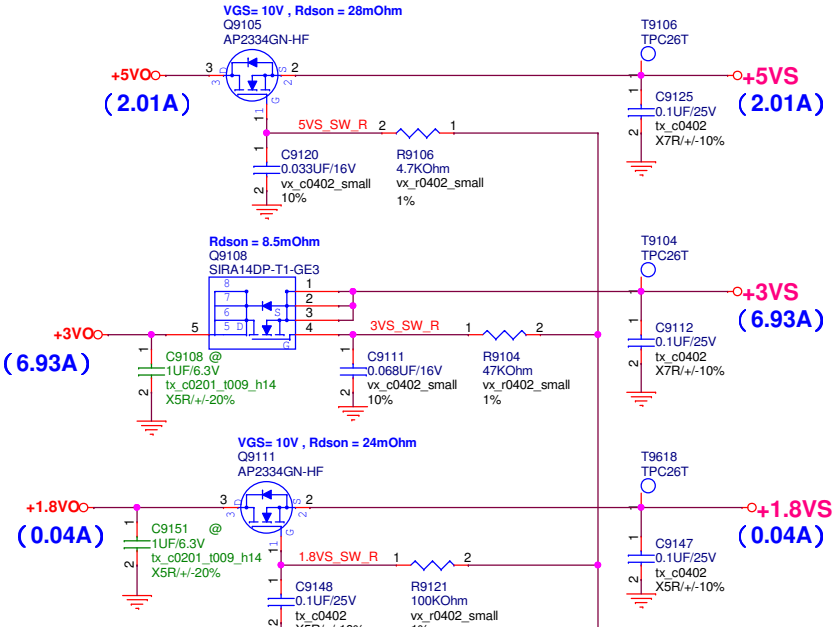
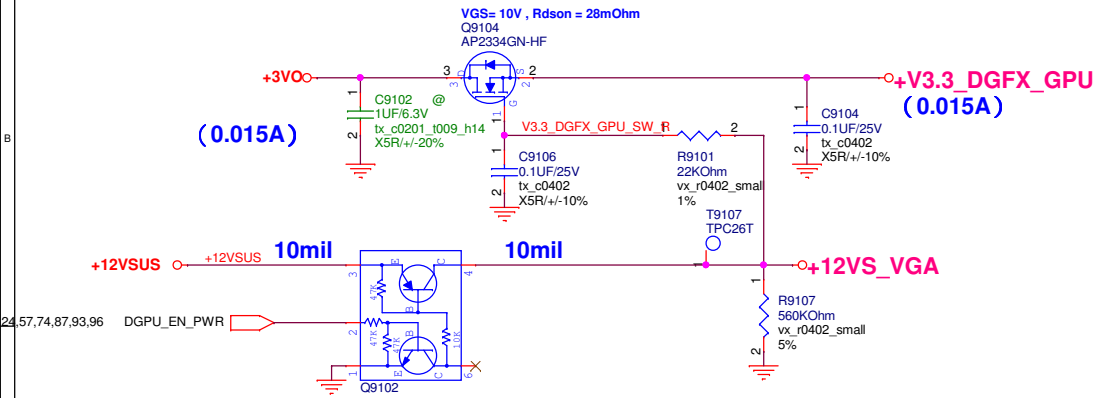
SUSC#_PWR POWER



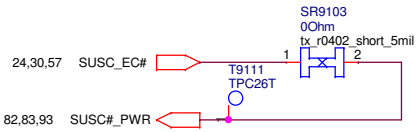
SUSB#_PWR POWER



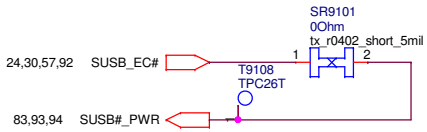
DGPU_EN_PWR POWER



SUSC#_PWR POWER Control



SUSB#_PWR POWER Control



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power_Load Switch

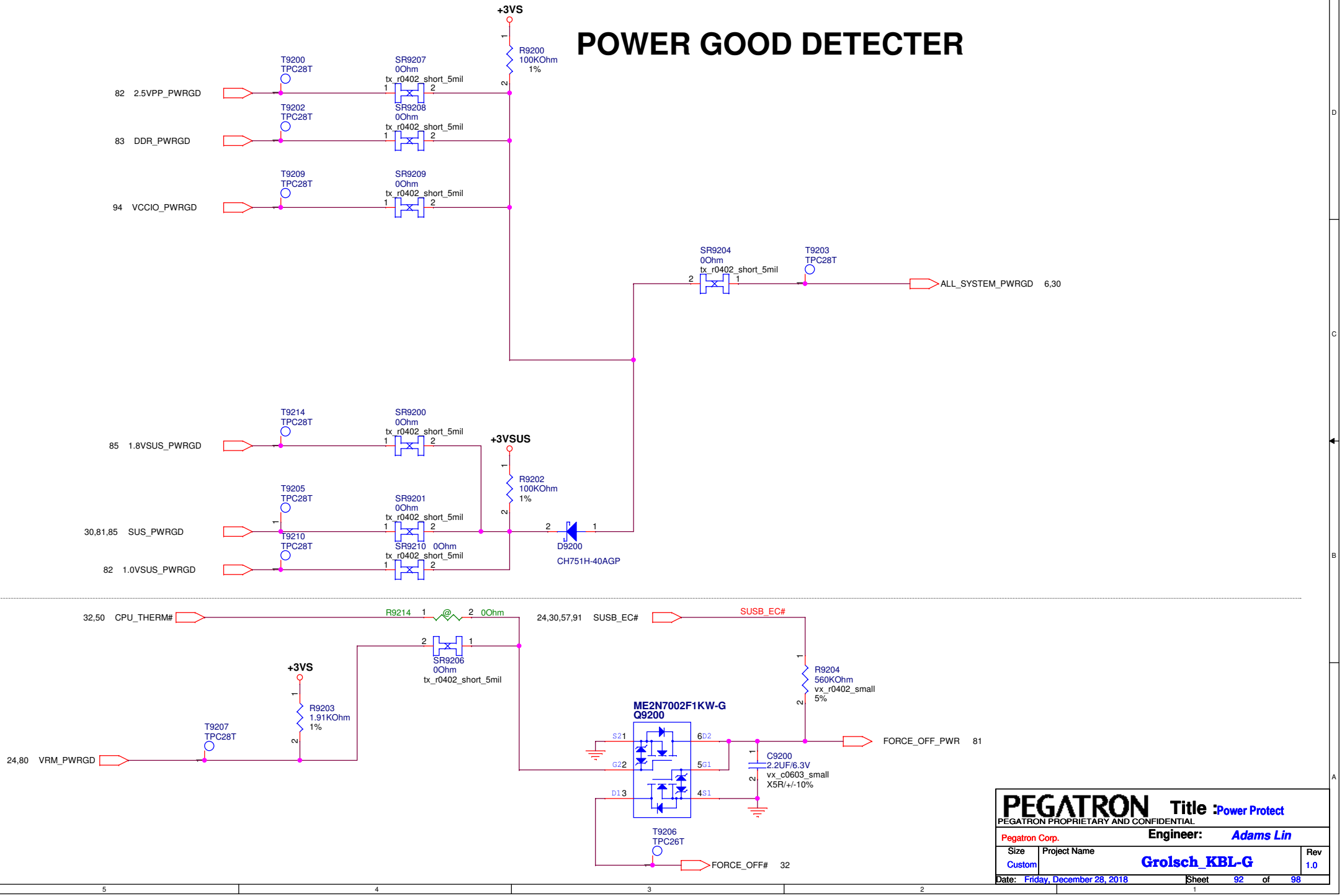
Pegatron Corp.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Friday, December 28, 2018 Sheet 91 of 98

POWER GOOD DETECTER



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power Protect

Pegatron Corp.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	Grolsch_KBL-G	1.0

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+AC_BAT_SYS → +AC_BAT_SYS 41,45,80,81,82,83,86,87,88,89,94
+BAT_CON → +BAT_CON 60,88
+AC_USBPD_WCT_IN → +AC_USBPD_WCT_IN 88,97

+5VA → +5VA 53,64,81
+3VA → +3VA 26,30,31,36,57,67,81,88

+5VO → +5VO 81,82,83,86,89,91,94
+3VO → +3VO 81,82,85,91,95,96
+2.5VO → +2.5VO 82
+1.8VO → +1.8VO 85,88,91
+1.2VO → +1.2VO 83
+1.0VO → +1.0VO 82,91
+0.95VO → +0.95VO 94
+5VSUS → +5VSUS 41,42,52,64,81
+3VSUS → +3VSUS 6,21,22,23,24,26,28,29,30,31,36,51,53,62,64,81,88,92
+1.8VSUS → +1.8VSUS 85,87
+1.0VSUS → +1.0VSUS 25,26,82

+3V → +3V 31,41,57,91
+1.2V → +1.2V 6,9,15,16,17,19,24,48,57,83
+1.0V → +1.0V 6,9,24,57,80,91
+2P5VPP → +2P5VPP 16,17,57,82

+VCORE → +VCORE 8,80
+VCCGT → +VCCGT 9,80
+VCCSA → +VCCSA 9,80
+VCCIO → +VCCIO 3,5,9,57,94

+0.85VO_VGA → +0.85VO_VGA 86
+V0.8_S → +V0.8_S 57,75,86
+VDDC → +VDDC 57,75,87
+VDD12 → +VDD12 7,57,75,87
+0.9VO_VGA → +0.9VO_VGA 89
+VDDCI → +VDDCI 57,75,89
+2.5VO_VGA → +2.5VO_VGA 95
+V2.5_HBM → +V2.5_HBM 57,74,75,95
+1.8VO_VGA → +1.8VO_VGA 57,74,96
+VDDIO_18 → +VDDIO_18 72,75,87,96
+VDDAN_18 → +VDDAN_18 7,75,96

+V3.3_DGFX_GPU → +V3.3_DGFX_GPU 24,57,72,73,74,75,91

+5VS → +5VS 31,36,41,48,50,57,64,69,80,87,91
+3VS → +3VS 6,21,22,23,24,26,30,31,32,36,41,42,44,45,48,50,51,53,57,62,64,73,87,91,92
+1.8VS → +1.8VS 22,36,57,74,91
+1.0VS → +1.0VS 9,57,91
+0.6VS → +0.6VS 15,57,83

+12VSUS → +12VSUS 60,91TS1#
+12V → +12V 91
+12VS → +12VS 31,91
+12VS_VGA → +12VS_VGA 91

FOR POWER TEST

+3VA

JP9300 SGL_JUMP 1 2 → T9300 TPC28T → CPU_VRON_PWR 80
JP9301 SGL_JUMP 1 2 → T9301 TPC28T → SUSB#_PWR 83,91,94
JP9302 SGL_JUMP 1 2 → T9302 TPC28T → SUSC#_PWR 82,83,91
JP9303 SGL_JUMP 1 2 → T9303 TPC28T → VSUS_ON 30,81,82,85
JP9304 SGL_JUMP 1 2 → T9304 TPC28T → DGPU_EN_PWR 24,57,74,87,91,96
JP9305 SGL_JUMP 1 2 → T9305 TPC28T → VDDCI_SVI2_VR_ON 74,87,89

BATTERY IN DETECT

+12VSUS → R9300 1KOhm vx_r0402_small 1% (2, 1) → BAT1_IN_OC# 30
C9300 @ 0.1UF/16V tx_c0402 X7R/+/-10% (2, 1)

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power Signal & Detect
Pegatron Corp.
Engineer: Adams Lin

Size	Project Name	Rev
Custom	Grolsch_KBL-G	1.0

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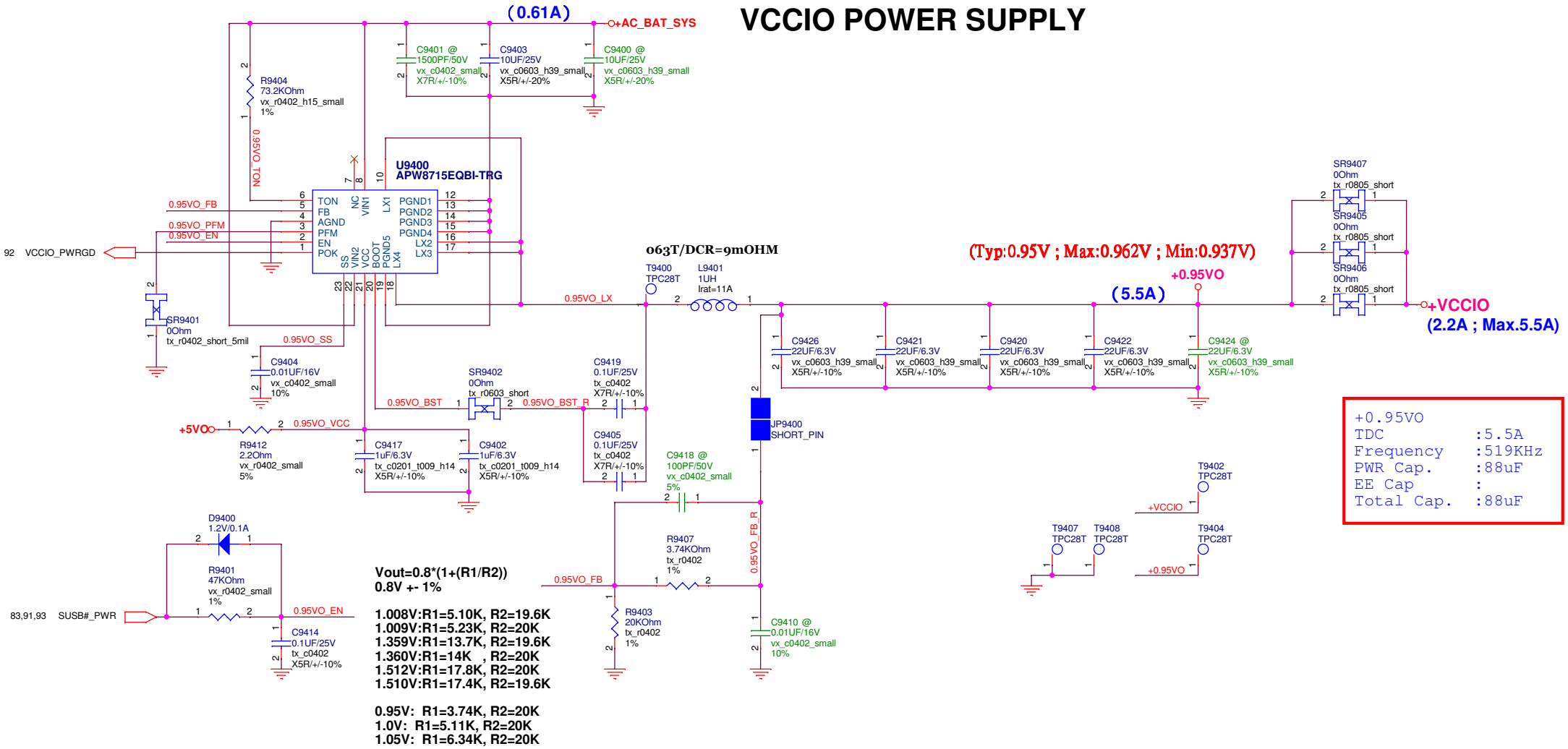
VCCIO POWER SUPPLY



Vout=0.8*(1+(R1/R2))
0.8V +- 1%

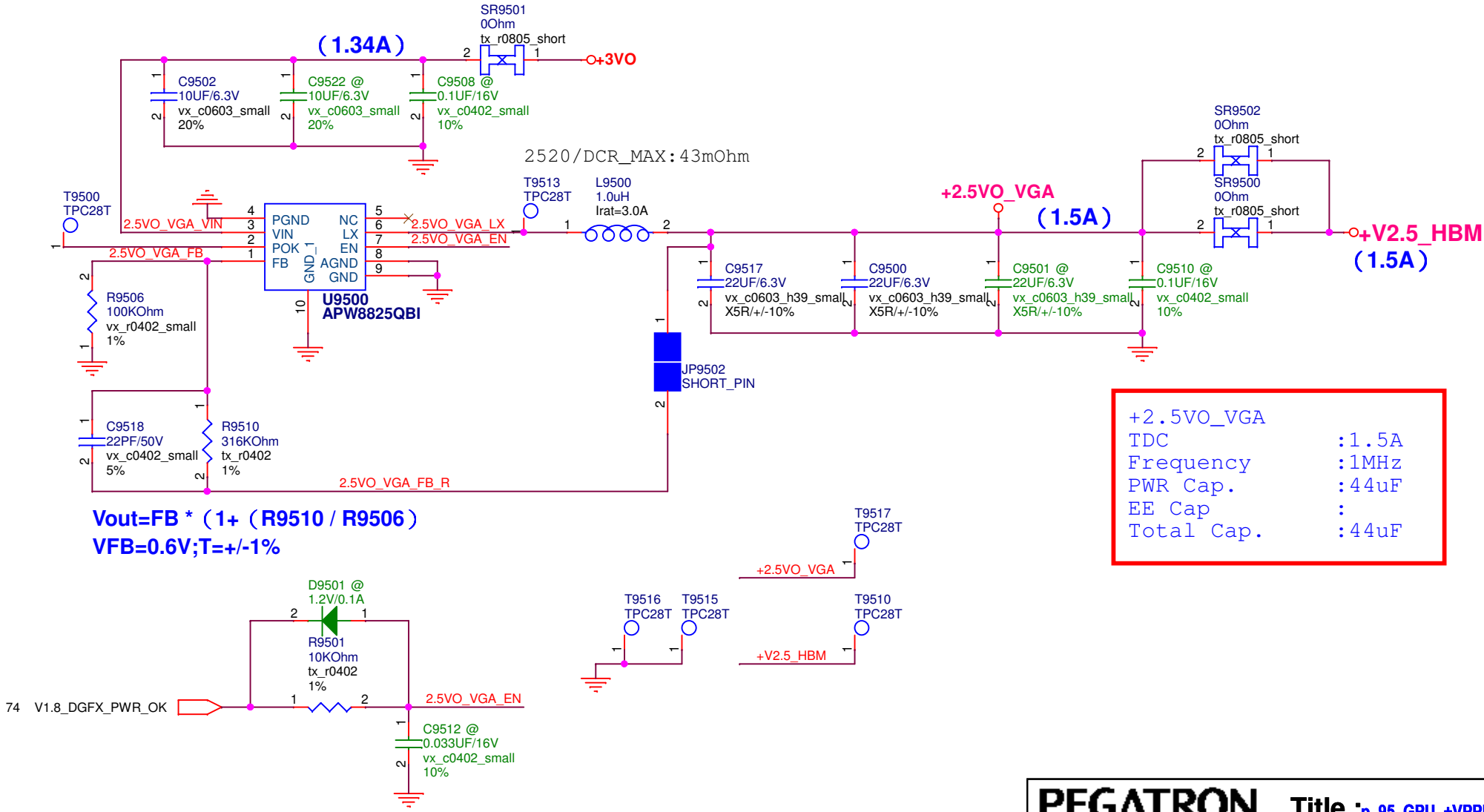
1.008V:R1=5.10K, R2=19.6K
1.009V:R1=5.23K, R2=20K
1.359V:R1=13.7K, R2=19.6K
1.360V:R1=14K , R2=20K
1.512V:R1=17.8K, R2=20K
1.510V:R1=17.4K, R2=19.6K

0.95V: R1=3.74K, R2=20K
1.0V: R1=5.11K, R2=20K
1.05V: R1=6.34K, R2=20K

+0.95VO	
TDC	:5.5A
Frequency	:519KHz
PWR Cap.	:88uF
EE Cap	:
Total Cap.	:88uF

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :Power_VCCIO
Pegatron Corp.
Engineer: Adams Lin
Size: Custom | Project Name: GS5FA | Rev: 1.0
Date: Friday, December 28, 2018 | Sheet 94 of 98

V2.5_HBM POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : p. 95_GPU_+VPPDC_2.5V

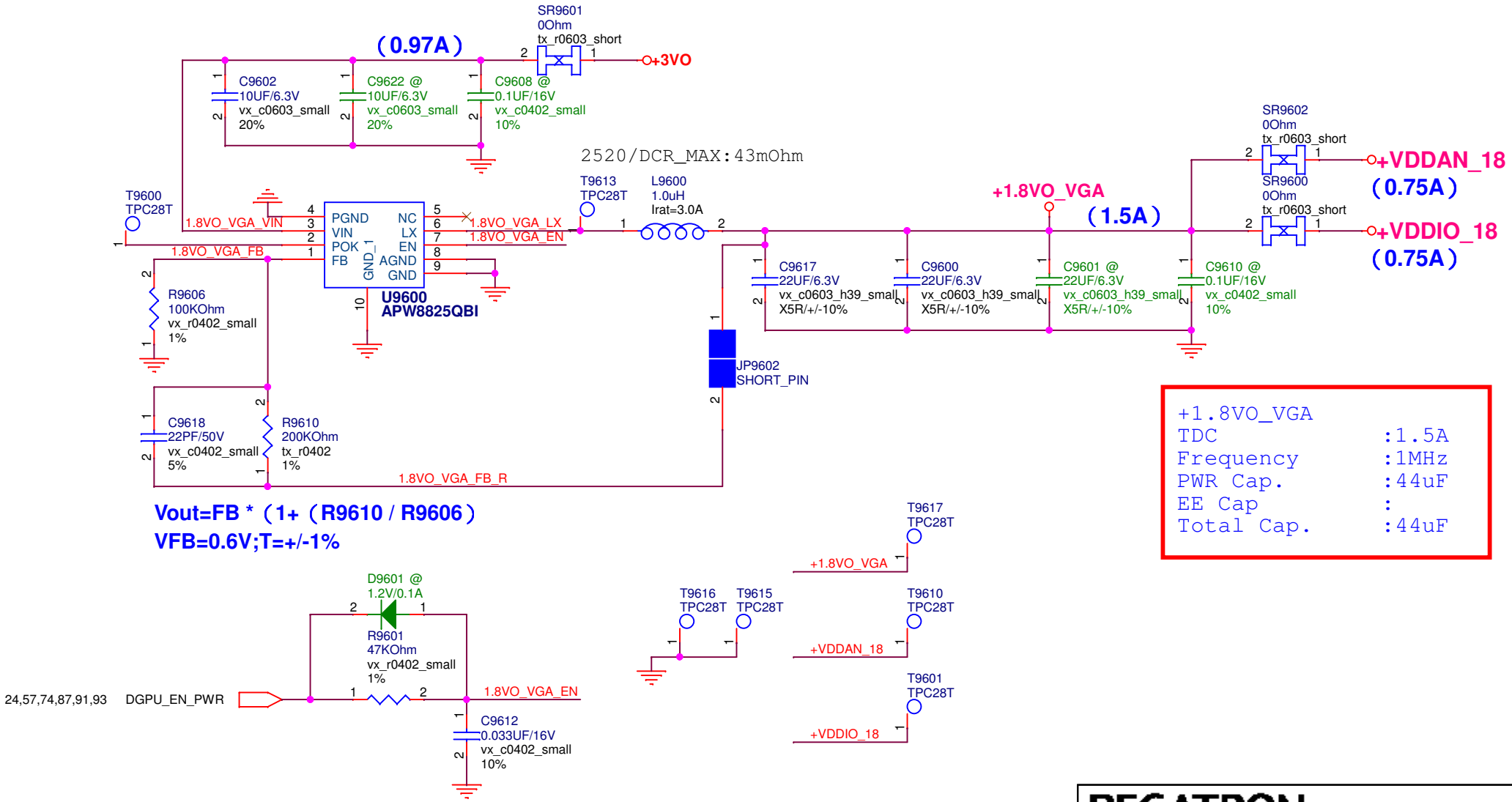
Pegatron Corp.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	Grolsch_KBL-G	1.0

Date: Friday, December 28, 2018 Sheet 95 of 98

VDDAN_18 & VDDIO_1.8V POWER SUPPLY



PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : Power_1.8VO_VGA

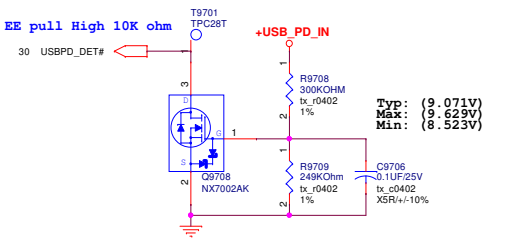
Pegatron Corp. Engineer: Adams Lin

Size	Project Name	Rev
Custom	GS5FA	1.0

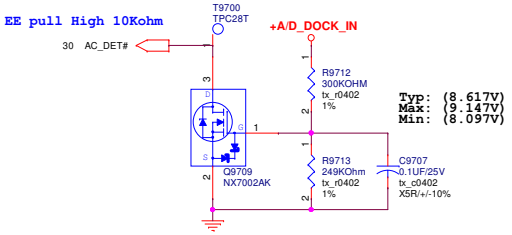
Date: Friday, December 28, 2018 Sheet 96 of 98

AC & USB_PD Detect

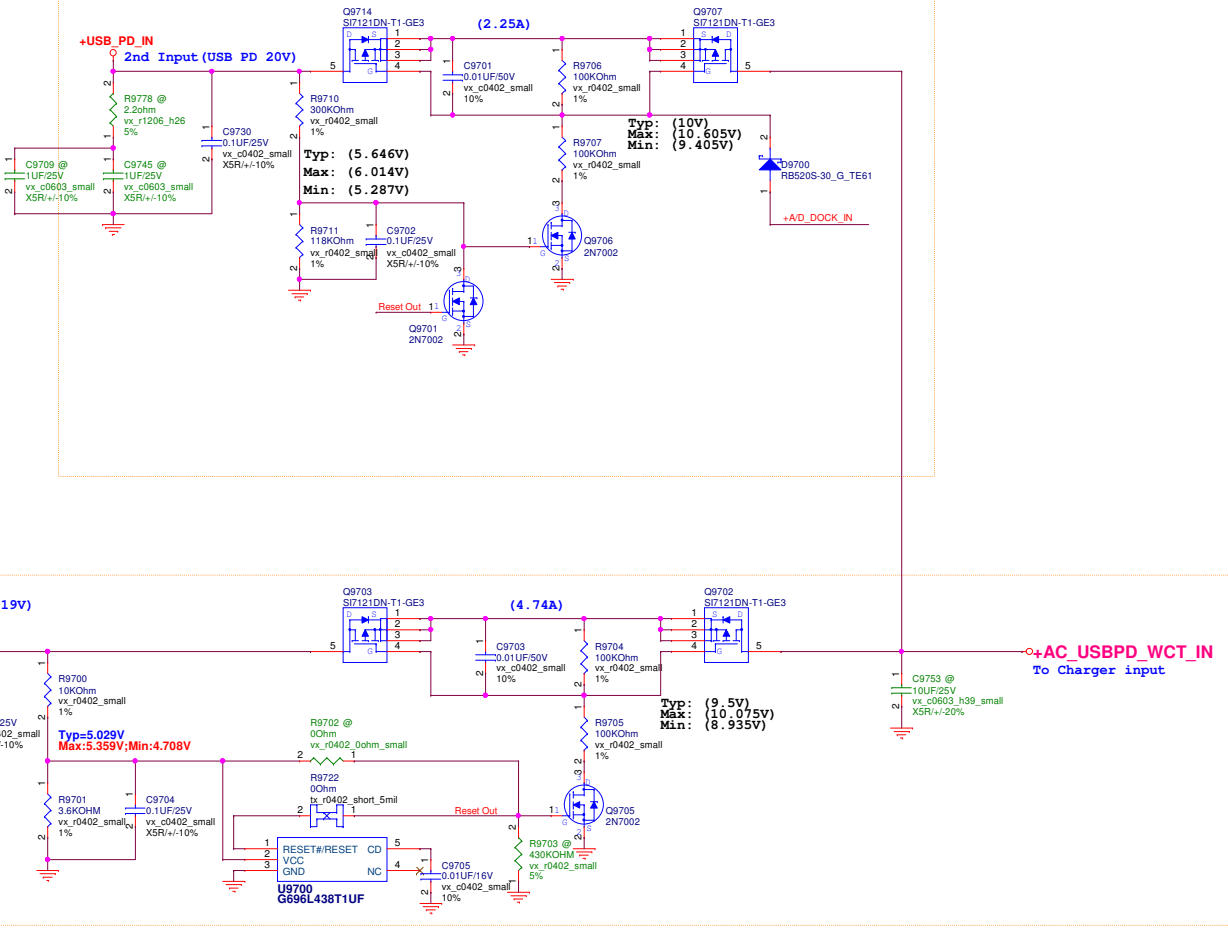
+USB_PD_IN DETECT 40W(5V~20V)



+A/D_DOCK_IN DETECT(90W,19V)



2 Input switch Circuit

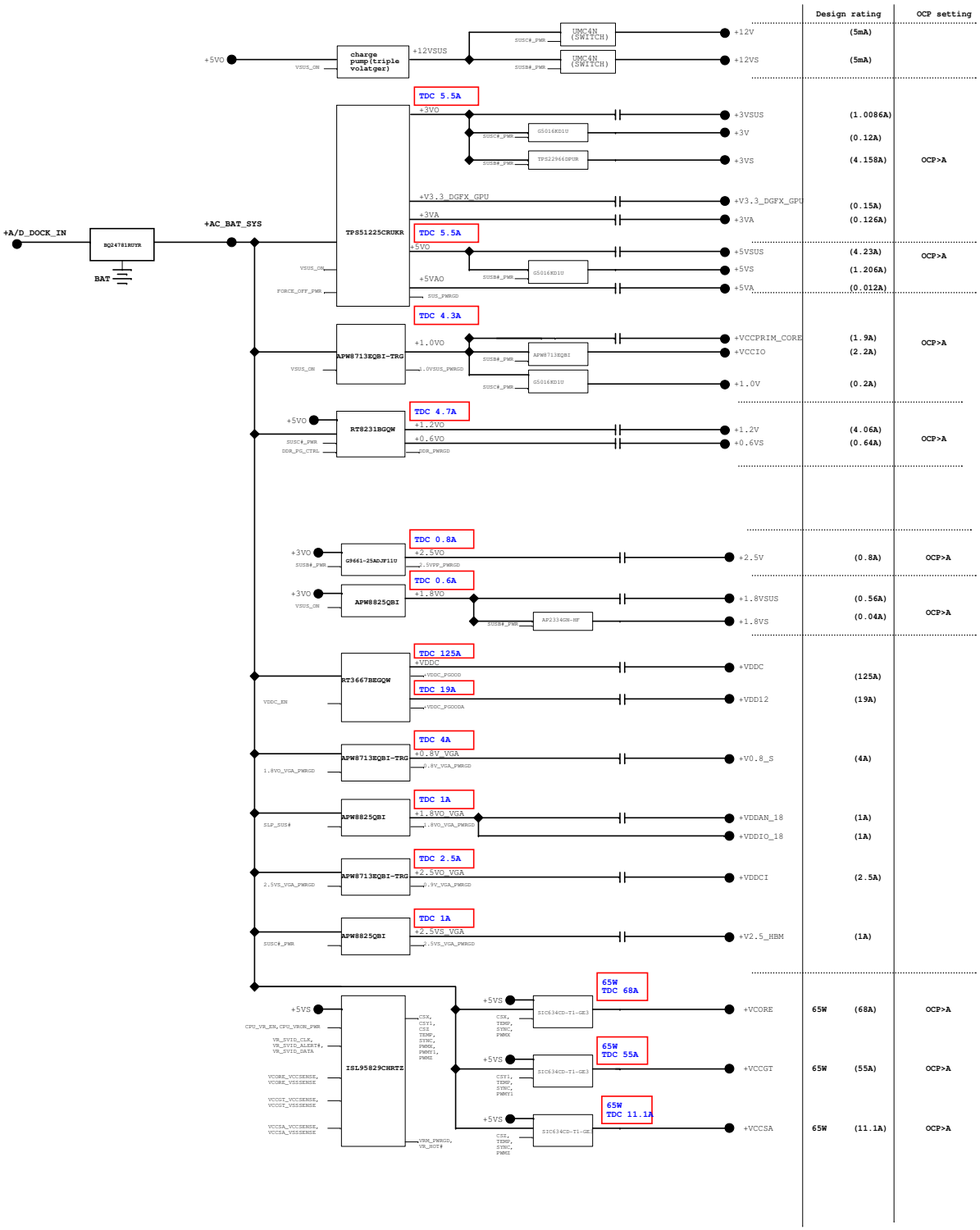


PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : Power_AC & PD S.W.
Engineer: Adams Lin

Size	Project Name	Rev
Custom	GS5FA	1.0

Date: Friday, December 28, 2018 Sheet 97 of 98



PEGATRON CORPORATION PROPRIETARY AND CONFIDENTIAL

Title : POWER_FLOWCHART

Engineer: Adams Lin

Size: Custom | Project Name: Grolsch_KHL-G | Rev: 1.0

Date: Friday, November 29, 2013 | Sheet 46 of 46